Prof. B. Rajendra Naik

Professor, Department of Electronics and Communication Engineering
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Osmania University, Hyderabad - 500007, Telangana, India
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Educational Qualifications

• B.Tech in Electronics and Communication Engineering, Nagarjuna University
• M.E. (Digital Systems), Osmania University
• Ph.D., Osmania University

Research IDs

Orcid ID: 0000-0002-9872-1433
Scopus ID: 57192573010
Vidwan ID: 242359
Google Scholar ID: 57192573010

Research Interests

VLSI signal processing, signal integrity and performance improvement of on-chip interconnects, image processing, machine learning, deep learning and edge AI for embedded/VLSI systems.

Research Projects

1. **Non-Invasive Measurement of Hemoglobin for Rural India using Artificial Intelligence Algorithms**

   Role: **Principal Investigator**
   Funding Agency: **SERB DST**
   Duration: **2019 - 2022**
   Project Cost (INR): **2217500**
   Status: **Completed**

2. **Advanced TERCOM Aided Inertial Navigation System by Velocity and Position Corrections**

Role: **Principal Investigator**
Funding Agency: **DRDO**
Duration: **2018 - 2020**
Project Cost (INR): **943000**
Status: **Completed**

3. **Research Project Seed money**

Role: **Principal Investigator**
Funding Agency: TEQIP-II
Duration: **2015 - 2016**
Project Cost (INR): **80000**
Status: **Completed**

Institute Level Scheme / Grant

1. **Visvesvaraya PhD scheme Phase-I**

Role: **Nodal Officer**
Funding Agency : **Ministry of Electronics & Information Technology (MeitY), Government of India**
Duration: **2017 - 2022**
Project Cost (INR): **21929000**
Status **Completed**

2. **Visvesvaraya PhD scheme Phase-II**

Role: **Nodal Officer**
Funding Agency : **Ministry of Electronics & Information Technology (MeitY), Government of India**
Duration: **2023 -2028**
Project Cost (INR): **11493600**
Status: **Ongoing**

Patents

1. **Non-Invasive Portable Device for Measuring Hemoglobin and Blood Pressure using Artificial Intelligence**
   Author: Rajendra Naik Bhukya
   Patent No. 512574 Status: Granted Year of Grant: 2024
2. **A Method and system for analyzing crosstalk noise in coupled On-Chip Interconnects**
   Authors: Rajendra Naik Bhukya and Bhaskar Gugulothu

Patent No. 2024/07831 Status: Granted Year of Grant: 2025

3. **3D Protective Mask Based Water quality Monitoring system powered by solar with good detection**
   Authors: Mr. A.Nageswara Rao, Dr. B.Rajendra Naik, Mr. G. Karthik Reddy, Dr. L. Nirmala Devi
   Patent No. 202141006261 Status: Published Year of Publication: 2021

Research Guidance:

Ongoing Ph.D. Candidates:

1. **L. Rajeshwar Reddy** -100520184006 - Deep learning based channel estimation with hybrid beamforming in millimeter wave massive MIMO systems.
2. **A. Harish Kumar -**100520204003 - A Design of Custom Architecture for Plant Leaves Classification and Disease Identification for Deep Learning using Convolution Neural Network.
3. **A. Sneha Keerthi** -100520234016 - Photoplethysmography based Machine Learning System for multivariate health monitoring.
4. **A. Sarada -**100520234017- Design of Efficient Memory based FIR Filters for Digital Signal Processing Applications

Ph.D. Awarded:

1. **Ravi Boda** (2020) - Machine Learning based Analysis and classification brain MRI Images
2. **Shoban Mude** (2020) - Novel Method for Performance Improvement in Polar Codes for communication system
3. **A. Nageswar Rao** (2021) - Energy Enhancement Heterogeneous Wireless Sensor Network to increase the Lifetime
4. **Bhaskar Gugulothu** (2022) - Performance Analysis of Signal Integrity for Carbon Nanotube On-Chip VLSI Interconnects using Multiresolution Time Domain Technique
5. **Raju Mudavath** (2022) - Signal Integrity analysis of Carbon Nanotube interconnects for high speed digital circuits
6. **K. Vijetha** (2023)- Design of low power low area distributed arithmetic based FIR filters
7. **C. Anil Kumar** (2023)- Novel Approaches for Secured Transmission of Images and Sensor Data using Compressive Sensing
8. **J. Praneeth Raj** (2024)-Analysis and Performance Improvement of Adaptive Beamforming Algorithms for Radar Applications

9. **R Padma Sree** (2024)- Improvement in the Quality of Services in Sub-6 GHz/mm Wave 5G Networks using equalizers and Decoupling of UL and DL with Machine Learning Approach

Professional Activities

- Visiting Researcher, Tokyo Metropolitan University, Tokyo, JAPAN (2010)
- Visited Japan (2023,2010,2009,2008), New Zealand (2019), Canada (2018), Switzerland (2017), Australia (2014), United Kingdom (2014) and Malaysia (2008) to present research papers in International Conferences.
- Professional Member of IEEE (Senior Member), IACSIT, SEEE.
- Delivered more than 30 expert lectures in the area of Digital systems and VLSI

Administrative Roles

- Director of PG colleges(2025 - till date)
- Dean, Students Affairs OU (2018 - till date)
- Nodal Officer, Visvesvaraya PhD Scheme, UCE OU (2016 to till date)
- Regional Coordinator, TGPSC (2024)
- Joint Director of Evaluation, Examination cell UCE OU (2017-2018)
- Head, Dept. of ECE (2014–2017 & 2019–2021)
- Secretary, Alumni Association UCE OU(2013-2015)
- Chairperson, Board of Studies (2012–2014)
- Coordinator, AP PGECET (2009)
- Coordinator, AP PGECET (2008–2011)
- PGECET Coordinator (2008-2011)
- Warden / Additional Chief Warden, College Hostels (2002–2017)

Courses Handled:

- Network Analysis and Synthesis
- VLSI Physical Design
- Digital Design and PLDs
- Digital VLSI Design
- IC Applications
- Basic Electronics
- Electronic Devices & Circuits
- Digital Image Processing
- Digital Image and Video Processing
- Digital Communications
- VLSI Design
- VLSI Design Technology
- Principles of VLSI System Design

Awards

- Best Teacher Award by Govt. of Telangana-2025
- Young Faculty Research Fellowship (YFRF) from MeitY, 2016.

Publications

Journals

1. Bhaskar Gugulothu, Rajendra Naik Bhukya, " Crosstalk Noise Modeling for Coupled SWCNT Bundle Interconnects using MRTD Technique" Scope Journal, Volume 14 Number 03, September 2024.
2. Mucherla Usha Rani, Siva Sankara Reddy N and Rajendra Naik B, " Design of reliable and fast Schmitt trigger 10T SRAM cells using in-memory computing" Engineering Research Express, Volume 6, Number 4, 2024.
   DOI 10.1088/2631-8695/ad80fd
3. Mucherla Usha Rani, N Siva Sankara Reddy, B Rajendra Naik, "A Read Delay Compensated and Write Assist Sram Cell with Power Gated and Power Delay Product Reduction Circuitry" e-Prime-Advances in Electrical Engineering, Electronics and Energy,2025.
   DOI: 10.1016/j.prime.2025.100950
4. Bhaskar Gugulothu, B Rajendra Naik, "Analysis of crosstalk noise in coupled MWCNT interconnects using MRTD technique", Microsystem Technologies,2024.
   DOI: 10.1007/s00542-024-05666-3
5. K Vijetha, B Rajendra Naik, "High-speed, low Area architecture of 2-D Block FIR Filter Using DA", Journal of Engineering Sciences,2023
   DOI: 10.10543/f0299.2021.41867
6. R Padmasree, B Rajendra Naik, "Improvement in the Quality of Services in Sub-6GHz/mm Wave Using Equalizers and Decoupling of UL and DL with Machine Learning Approach", Journal of Communications,2023
   DOI: 10.12720/jcm.18.9.599-607
7. AmgothLaxman, N Siva Sankara Reddy, B Rajendra Naik, "Design and implementation of hybrid logic based MAC unit using 45 nm technology", e-Prime-Advances in Electrical Engineering, Electronics and Energy,2023
   DOI: 10.1016/j.prime.2023.100317
8. D Srinivas, N Siva Sankara Reddy, B Rajendra Naik, "Design and analysis of hybrid 10T adder for low power applications", e-Prime-Advances in Electrical Engineering, Electronics and Energy,2023.
   DOI: 10.1016/j.prime.2023.100379
9. MalihaNaaz, Kaleem Fatima, B Rajendra Naik, Mohammad Ibrahim, AsfiyaJabeen, Syed Junaid Hussain, "A DC-DC Boost Converter using PWM

with 65% efficiency", 2023 IEEE Devices for Integrated Circuit,2023
DOI: 10.1109/DevIC57758.2023.10134808

10. MalihaNaaz, Kaleem Fatima, B Rajendra Naik, Shaik Abu Anzar Sayeed, Syed Saquib Ahmed, Mohammed ShahzaibAshher**,** "Design of DC-DC Boost Converter Using PFM Switching Technique", 2023 IEEE Devices for Integrated Circuit (DevIC),2023.
DOI: 10.1109/DevIC57758.2023.10134869
11. Sangeeta Singh, JVR Ravindra, B RajendraNaik, " Proffering Secure Energy Aware Network-On-Chip (Noc) Using Incremental Cryptogine**",** Sustainable Computing: Informatics and Systems,2022.
DOI: 10.1016/j.suscom.2022.100682
12. Sangeeta Singh, JVR Ravindra, B RajendraNaik, "Design and Analysis of a Novel Low Complexity and Low Power Ping Lock Arbiter by using EGDI based CMOS Technique", International Journal of Integrated Engineering,2022.
DOI: 10.30880/ijie.2022.14.01.034
13. Sangeeta Singh, JVR Ravindra, B RajendraNaik, "Design and Analysis of a Novel Low Complexity and Low Power Ping Lock Arbiter by using EGDI based CMOS Technique", International Journal of Integrated Engineering,2022
14. Bhaskar Gugulothu, Rajendra Naik Bhukya, **"**Crosstalk noise analysis of coupled on-chip interconnects using a multiresolution time domain (MRTD) technique", Journal of Computational Electronics,Volume 21, Issue 1,Pages 348 - 359,2022.
DOI: 10.1007/s10825-021-01828-y
15. Anil Kumar Chatamoni, RajendraNaikBhukya, "Lightweight Compressive Sensing for Joint Compression and Encryption of Sensor Data", International Journal of Engineering and Technology,vol. 12, no. 2, pp. 167-181 ,2022.
DOI: 10.46604/ijeti.2022.8599
16. Sangeeta Singh, JVR Ravindra, B Rajendra Naik, "Design and implementation of network‐on‐chip router using multi‐priority based iterative round‐robin matching with slip", Transactions on Emerging Telecommunications Technologies,2022.
DOI: 10.1002/ett.4514
17. Sangeeta Singh, JVR Ravindra, B Rajendra Naik, "Prediction of Intermittent Failure by Presage Debacle Model in Network on Chip", International Journal of Computer Network and Information Security,PP.75-88,2022.
DOI: 10.5815/ijcnis.2022.04.06
18. Praneet Raj Jeripotula, B Rajendra Naik, Raju Mudavath, "A Novel Hybrid Weighted Method-Based Beamforming for Sidelobe Level Reduction in Radar Applications", Arabian Journal for Science and Engineering,Volume 47, pages 14133–14145, 2022.
DOI: 10.1007/s13369-022-06656-1

19. Jeripotula, Praneet Raj, C. Anil Kumar, and B. RajendraNaik, "A novel sign variable step size LMS (SiVSS-LMS) algorithm for adaptive beamforming", CSI Transactions on ICT,2020.
DOI: 10.1007/s40012-020-00313-4
20. K Vijetha, B RajendraNaik, "High performance area efficient DA based FIR filter for concurrent decision feedback equalizer", International Journal of Speech Technology **23**, 297–303 (2020).
DOI: 10.1007/s10772-020-09695-x
21. Praneet Raj Jeripotula, C Anil Kumar, MudavathRaju, B RajendraNaik, "A novel algorithm design for adaptive beamforming in uniform linear array antenna", J. Mech. Continua Math. Sci,2020.
DOI: 10.26782/jmcms.2020.03.00008
22. BhaskarGugulothu, RajendraNaikBhukya, "Transient Analysis of Crosstalk Noise Effects in SWCNT Bundle On-Chip Interconnects Using MRTD Technique"**,** ECS Journal of Solid State Science and Technology,2021
DOI:10.1149/2162-8777/ac2e7e
23. RajuMudavath, BhukyaRajendraNaik, JeripotulaPraneet Raj, "Evaluation and reduction of signal integrity issues in multiwalled carbon nanotube on-chip VLSI interconnects", ECS Journal of Solid State Science and Technology,2021
DOI: 10.1149/2162-8777/ac1c5b
24. Anil Kumar Chatamoni, RajendraNaikBhukya, Praneet Raj Jeripotula, "A Novel Approach based on Compressive Sensing and Fractional Wavelet Transform for Secure Image Transmission", International Journal of Intelligent Engineering and Systems,Vol.14, No.4,2021.
DOI: 10.22266/ijies2021.0831.02
25. RajuMudavath, RajendraNaikBhukya, Praneet Raj Jeripotula, "The mitigation of signal integrity issues in coupled MWCNT bundles and a comparison with Cu interconnects", Journal of Computational Electronics **20**, 1430–1438 (2021).
DOI: 10.1007/s10825-021-01684-w
26. G Aparna, RaparlaSwathi, M Kezia Joseph, CN Sujatha, B RajendraNaik, "FPGA implementation of polar codes for 5G eMBB control channels", International Journal of Ultra Wideband Communications and Systems,2021
DOI: 10.1504/IJUWBCS.2021.119139
27. M. Venkata Ramanaiah, Sudhakar Alluri, B. Rajendra Naik, N.S.S.Reddy, "Transistor sizing of CMOS VLSI Circuits in Deep Submicron Technology"International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume-8, Issue-11S2, pp15-29, September 2019.
DOI: 10.35940/ijitee.K1004.09811S219
28. Sudhakar Alluri, N.S.S.Reddy, B.Rajendra Naik, "Low Power, High Speed and Low Area of Fin FET 4:1Multiplexer VLSI Circuit Design in 18nm Technology"

International Journal of Recent Technology and Engineering (IJRTE), Volume-8, Issue-3, pp 1369-1372, September 2019.
DOI:10.35940/ijrte.B3395.098319

29. Praneet Raj Jeripotula, C Anil Kumar, B Rajendra Naik, "Modified leaky LMS algorithm for adaptive beamforming" International Journal of Engineering, Applied and Management Sciences Paradigms (IJEAM), Volume 54 Issue 3, ISSN 2320-6608, June 2019
30. Rajendra Naik Bhukya, Raju Mudavath "Analysis and minimization of crosstalk noise in copper interconnects for high-speed VLSI circuits" CSI Transactions on ICT, Volume 7, Issue 2, pp 81–86, June 2019.
DOI:10.1007/s40012-019-00243-w
31. Shoban Mude, Rajendra Naik Bhukya "Minimization of Bit Error rate in Polar Codes for Achieving Channel Capacity" International Journal of Engineering and Advanced technology, Volume-IX, Issue I, pp 1433-1436, 2019.
DOI:10.35940/ijeat.A1233.109119
32. Sudhakar Alluri, B Rajendra Naik, NSS REDDY, M Venkata Ramanaiah, "Fin FET Two Bit Comparator for Low Voltage, Low Power, High Speed and Low Area in 18nm Technology" International Research Journal of Engineering and Technology (IRJET), e-ISSN: 2395-0056, p-ISSN: 2395-0072, 2019
33. Ravi Boda, B. Rajendra Naik "Magnetic Resonance Imaging Rician Noise Reduction using Advance Wavelet Transform and Nonlocal Mean Filter" International Journal of Imaging & Robotics, Volume 19, Issue 3, 2019.
34. Shoban Mude, B. Rajendra Naik "Channel Estimation for MIMO based-Polar Codes" International Journal of Advance Engineering and Research Development, Volume 5, Issue 1, pp 841-845, January 2018.
35. Ravi Boda, B. Rajendra Naik, D. Srinivas, Boda Aruna "Timing Analysis of Noisy MRI Segmentation using modified Watershed Algorithm" International Journal of Emerging Technology and Advanced Engineering, Volume 7, Issue 12, pp 89-95, December 2017.
36. Ravi Boda, B. Rajendra Naik, D Srinivas, Boda Aruna "Brain MR Image Segmentation using Coherent Local Intensity Clustering Phenomena" International Journal of Advance Engineering and Research Development Volume 4, Issue 12, pp 419- 424, December -2017.
37. Pasala Raja Prakasha Rao, B. Rajendra Naik "An Efficient Power Delay Product of ZigBee Transmitter Using Verilog HDL" IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), Volume 12, Issue 3, 2017, pp 18-26,
DOI: 10.9790/2834-1203041826
38. Sudhakar Alluri, M.Dasharatha, B. Rajendra Naik, N. S. S. Reddy "Optimization of Voltage, Delay, Power and Area for 16-bit Cyclic Redundancy Check (CRC) in

VLSI Circuits using 45nm Technology" Int. Journal of Engineering Research and Application, Volume 7, Issue 9, pp.78-84, September 2017.
DOI:10.9790/9622-0709077884

39. Sudhakar Alluri, M.Dasharatha, B. Rajendra Naik, N. S. S. Reddy "Design and Estimation of Power, Delay and Area for Parallel Adder in VLSI Circuits using 45nm Technology" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 7, Issue 4, pp 56-65, Jul-Aug 2017.
DOI:10.9790/4200-0704025665
40. Raja Prakasha Rao Pasala, Rajendra Naik Bhukya, "A Comprehensive Analysis of Design and Simulation of Power Optimized CRC Algorithm for ZIGBEE Application" International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 Vol. 6 Issue 04, April-2017.
41. Sudhakar Alluri, B Rajendra Naik, NSS REDDY, "Design of Second Order Adiabatic Logic for Energy Dissipation in VLSI CMOS Circuits" SSRG International Journal of VLSI & Signal Processing (SSRG-IJVSP) – Volume 4 Issue 1 Jan to April 2017
DOI: 10.14445/23942584/IJVSP-V4I1P103
42. Pasala Raja Prakasha Rao, Dr.B.Rajendra Naik, "Verilog Based Design and Simulation of MAC and PHY Layers for Zigbee Digital Transmitter " Pasala Raja Prakasha Rao Int. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 4, Issue 12(Part 5), pp.09-17, December 2014.
43. RK Niranjan, B Rajendra Naik, " Approach of pulse parameters measurement using digital IQ method" International Journal of Information and Electronics Engineering, Volume 4, Issue 1,Pages 31, 2014.
10.7763/IJIEE.2014.V4.403
44. P Prashanti, B Rajendra Naik, "Design and Implementation of High Speed Carry Select Adder" International Journal of Engineering Trends and Technology (IJETT), Volume 4, Issue 9, Pages 3985-3990, 2013.
DOI: 10.17577/IJERTV4IS020383
45. Gonuguntla, H.K., Rao, P. & Naik, B. Asthma diagnosis and treatment – 1011. OZAC- a herbal medicine for bronchial asthma. Gonuguntla et al. World Allergy Organization Journal 2013, 6 (Suppl 1), P11 (2013).
DOI: 10.1186/1939-4551-6-S1-P11
46. B. Rajendra Naik and Rameshwar Rao , "Optimization of Power and Area in Self-Checking Carry-Select Adder Design based on Two-Rail Encoding" International Journal of Engg. Research & Indu. Appls. (IJERIA), ISSN:09741518, Vol.2 ,No.VII (2009), pp 329-346.
47. Pasala Raja Prakasha Rao, B Rajendra Naik, "A Comprehensive Analysis of Literature Reported Mac and PHY Enhancements of ZigBee and Its Alliances"

International Journal on Recent and Innovation Trends in Computing and Communication, Volume 4, Issue 1, Pages 219-233, 2001.
DOI: 10.17762/ijritcc.v4i1.1737

Conferences

1. A Laxman, NSS Reddy, BR Naik , "Area and Power Efficient Design of Novel Karatsuba Double MAC (K-DMAC)" International Conference on Inventive Research in Computing Applications,pp. 103-108, 2022.
   DOI: 10.1109/ICIRCA54612.2022.9985758
2. Rajeshwar Reddy, Rajendra Naik Bhukya, "A Comprehensive Survey on mm Wave Systems with Beamforming Effects in Antenna for 5G Applications", International Conference on Trends in Electronics and Informatics,pp. 504-509, 2022.
   DOI: 10.1109/ICOEI53556.2022.9777176
3. A Harish Kumar, B RajendraNaik, "The Performance Analysis and comparison of Machine Learning Classifiers and Neural Network on Crop Recommendation", International Conference on Advanced Computing and Communication Systems, pp. 811-815, 2022.
   DOI: 10.1109/ICACCS54159.2022.9785065
4. Bhaskar Gugulothu, B RajendraNaik, "Analysis of Signal Integrity in Coupled MWCNT and Comparison with Copper Interconnects", International Conference for Advancement in Technology, pp.1-5, 2022.
   DOI: 10.1109/ICONAT53423.2022.9726011
5. A Nageswar Rao, B Rajendra Naik, L Nirmala Devi, K VenkataSubbareddy, "Trust and Packet Loss Aware Routing (TPLAR) for Intrusion Detection in WSNs", 2020 12th International Conference on Computational Intelligence and Communication Networks (CICN), Bhimtal, India, pp. 386-391, 2020.
   DOI: 10.1109/CICN49253.2020.9242621
6. Rajendra Naik Bhukya, Swetha Kodepaka, Vennela Dharavath, Ravi Boda, "Position and Velocity Errors Reduction Using Advanced TERCOM Aided Inertial Navigation System", International Conference on Innovative Computing and Communications,2021.
   DOI: 10.1007/978-981-15-5113-0_67
7. RN Bhukya, S Mude, G Sneha, "Non-invasive Measurement of Oxygenated Haemoglobin (SpO 2) and Blood Pressure", Advances in Clean Energy Technologies,2021
   DOI: 10.1007/978-981-16-0235-1_5
8. M Sushma Sri, B RajendraNaik, K Jayasankar, B Ravi, P Praveen Kumar, "On the Use of Region Convolutional Neural Network for Object Detection", Data Engineering and Communication Technology,2021.

DOI: 10.1007/978-981-16-0081-4_31

9. Rajendra Naik Bhukya, Swetha Kodepaka, Vennela Dharavath, Ravi Boda, "Position and Velocity Errors Reduction using Advanced TERCOM Aided Inertial Navigation System" International Conference on Innovative Computing and Communication (ICICC- 2020), 21 -23 February 2020, Delhi.

   DOI: 10.1007/978-981-15-5113-0_67

10. M. Sushma Sri, B. Rajendra Naik, K. Jayasankar "Object Tracking using Motion Estimation based on Block Matching Algorithm" International Conference on Inventive Computation Technologies (ICICT), 26-28 Feb. 2020, Coimbatore, India, ISBN:978-1-7281-4685-0

    DOI: 10.1109/ICICT48043.2020.9112511

11. M. Sushma Sri, B. Rajendra Naik, K. Jayasankar, "Edge Detection Using Block Processing and Lookup Table" International Conference on Communication and Electronics Systems (ICCES),10-12 June 2020, COIMBATORE, India, ISBN: 978-1-7281-5371-1

    DOI: 10.1109/ICCES48766.2020.9137978

12. Shoban Mude, Rajendra Naik Bhukya, "Polar Code and Polarization using Bhattacharya Parameter" IEEE Annual Information Technology, Electronics and Mobile Communication Conference, 17-19 October, 2019, Vancouver, BC, Canada, ISBN: 978-1-5386-7266

    DOI: 10.1109/IEMCON.2018.8615026

13. Dasharatha, M., Rajendra Naik, B., Reddy, N.S.S., Mude, S. (2020). VLSI Design and Synthesis of Reduced Power and High Speed ALU Using Reversible Gates and Vedic Multiplier. In: Satapathy, S.C., Raju, K.S., Shyamala, K., Krishna, D.R., Favorskaya, M.N. (eds) Advances in Decision Sciences, Image Processing, Security and Computer Vision. ICETE 2019. Learning and Analytics in Intelligent Systems, vol 4. Springer, Cham.

    DOI: 10.1007/978-3-030-24318-0_33

14. Bhaskar Gugulothu, B.Rajendra Naik, Sampath Boodidha, "Modeling of Capacitive Coupled Interconnects for Crosstalk Analysis in High Speed VLSI Circuits" IEEE International Conference on Communication and Signal Processing – ICCSP2019, 4-6 April 2019, Chennai, India, ISBN:978-1-5386-7595-3

    DOI: 10.1109/ICCSP.2019.8697925

15. Raju Mudavath, B. Rajendra Naik, Bhaskar Gugulothu, "Analysis of Crosstalk Noise for Coupled Microstrip Interconnect Models in High-Speed PCB Design"

International Conference on Electronics, Information,and Communication (ICEIC) 22-25 Jan 2019 Pullman Auckland, New Zealand, ISBN:978-89-950044-4-9

DOI: 10.23919/ELINFOCOM.2019.8706385

16. Praneet Raj, Jeripotula, B.Rajendra Naik, "Performance Analysis of Adaptive Beamforming Algorithms" IEEE International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET), 21-22, December 2018,Kottayam, India, ISBN:978-1-5386-0576-9

    DOI: 10.1109/ICCSDET.2018.8821132

17. C. Anil Kumar, B. Rajendra Naik, "A new encrypted image watermarking based on DTCWT and random pixel exchange" International Conference on Advanced Computing & Communication Systems (ICACCS), 15-16 March 2019, Coimbatore, Tamil Naidu, India, ISBN: 978-1-5386-9533-3

    DOI: 10.1109/ICACCS.2019.8728398

18. C. Anil Kumar, B. Rajendra Naik, "Image Security with Compressive Sensing and Fractional Wavelet Transform" IEEE Third International Conference on Circuits, Control, Communications and Computing(I4C-2018), 3-5 October 2018, Bangalore, India, ISBN:978-1-5386-8487-0

    DOI: 10.1109/CIMCA.2018.8739702

19. Raju Mudavath, B. Rajendra Naik, "Estimation of Far End Crosstalk and Near End Crosstalk Noise with Mutually Coupled RLC Interconnect Models"IEEE International Conference on Communication and Signal Processing, 3-5 April 2018, Chennai, India, ISBN:978-1-5386-3521-6

    DOI: 10.1109/ICCSP.2018.8524191

20. B.RajendraNaik, A.Nageshwar Rao, "Elastic investigation on LEACH, Hetro-LEACH,SEP and NHSEP routing protocols in wireless sensor networks" International conference on communication and network technology (ICCNT-2017), September 1-3, 2017, Zurich, Switzerland.
21. B. Rajendra Naik, G.Bhaskar, "Design and Implementation of LUT Based FPGAs" International multidisciplinary conference on "Education for Future: Issues and Challenges" 8–9July, 2017, Osmania University, Hyderabad, India.
22. A. Vijendar, Ravi Boda, P Ram Kumar, B.Rajendra Naik, "Image Compression Using Adaptively Scanned Wavelet Difference Reduction Technique (ASWDRT)" IEEE International Conference on Intelligent Computing and Control Systems ICICCS-2017, June 15-16 2017, Madurai, India.

    DOI: 10.1109/ICCONS.2017.8250643

23. S. Mude, M. Dasharatha and B. R. Naik, "High-throughput and energy-efficient SCL decoder design using FPGA," 2017 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 2017, pp. 0395-0399.

    DOI: 10.1109/ICCSP.2017.8286385

24. Shoban Mude, B Rajendra Naik, “EDA Design in VLSI Using Coding Techniques” 2017 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 2017
25. M. Dasharatha, B. R. Naik and N. S. S. Reddy, "Low power and area efficient FIR filter using adaptive LMS algorithm," 2017 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 2017, pp. 0453-0456.

    DOI: 10.1109/ICCSP.2017.8286398

26. M Dasharatha, Shoban Mude, B RajendraNaik, NSS Reddy, “Design of a low power adaptive LMS filter for filtering different input signals” ICCSP-2017, Chennai, India, 2017
27. R. Boda and B. R. Naik, "A novel bias field analysis and classification of MR images," 2017 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 2017, pp. 0188-0193.

    DOI: 10.1109/ICCSP.2017.8286812

28. B Rajendra Naik, Ravi Boda, “A Modified Bias Field Estimation and Classification of Medical Images” International Conference on Systemics, Cybernetics and Informatics, March 2017.
29. S. Singh, J. Ravindra and B. R. Naik, "Power and area calibration of switch arbiter for high speed switch control and scheduling in network-on-chip," 2016 International SoC Design Conference (ISOCC), Jeju, Korea (South), 2016, pp. 5-6.

    DOI: 10.1109/ISOCC.2016.7799765

30. S. Mude and B. R. Naik, "High speed low power wireless signal timing analysis on FPGA using turbo coding and Viterbi algorithm," 2016 1st India International Conference on Information Processing (IICIP), Delhi, India, 2016, pp. 1-4.

    DOI: 10.1109/IICIP.2016.7975300

31. S. Alluri, M. Dasharatha, B. R. Naik and N. S. S. Reddy, "Design of low power high speed full adder cell with XOR/XNOR logic gates," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, 2016, pp. 0565-0570.

    DOI: 10.1109/ICCSP.2016.7754203

32. S. Mude and B. R. Naik, "High performance wireless system by using VA and GA selection," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, 2016, pp. 0342-0345.

    DOI: 10.1109/ICCSP.2016.7754152

33. R. Boda, S. K. Yezerla and B. R. Naik, "Performance analysis of image segmentation methods for noisy MRI images," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, 2016, pp. 0942-0946.

    DOI: 10.1109/ICCSP.2016.7754286

34. S. Alluri, B. R. Naik and N. S. S. Reddy, "Mapping of five input wallace tree using cadence tool for low power, low area and high speed," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, 2016, pp. 0304-0310.

    DOI: 10.1109/ICCSP.2016.7754144

35. R. K. Niranjan and B. R. Naik, "FPGA based implementation of pulse parameters measurement," 2014 Science and Information Conference, London, UK, 2014, pp. 862-867.

    DOI: 10.1109/SAI.2014.6918286

36. S. K. Yezerla and B. Rajendra Naik, "Design and estimation of delay, power and area for Parallel prefix adders," 2014 Recent Advances in Engineering and Computational Sciences (RAECS), Chandigarh, India, 2014, pp. 1-6.

    DOI: 10.1109/RAECS.2014.6799654

37. B Rajendra Naik, Rameshwar Rao, S Shefail, “Low-area low-power and high-speed TCAMS” International Conference on VLSI, Communication and Instrumentation (ICVCI), 2011.
38. B. R. Naik, R. Rao and P. Chandrasekhar, "Design of 12-bit, 1.8V current steering digital-to-analog converter," 2008 International Conference on Electronic Design, Penang, Malaysia, 2008, pp. 1-6

    DOI: 10.1109/ICED.2008.4786676

39. B. Rajendra Naik, R. Rao and P. Chandrasekhar, "Design of SRAM with sleep transistor for leakage reduction," 2008 International Conference on Electronic Design, Penang, Malaysia, 2008, pp. 1-6

    DOI: 10.1109/ICED.2008.4786662

Book Chapters

1. Rajendra Naik Bhukya, Shoban Mude , G. Sneha, “Non-invasive Measurement of Oxygenated Hemoglobin (SpO_2) and Blood Pressure” chapter in Advances in Clean Energy Technologies (Springer Proceedings in Energy), 2021.
   DOI: 10.1007/978-981-16-0235-1_5
2. Sudhakar Alluri, B. Rajendra Naik, N. S. S. Reddy, M. Venkata Ramanaiah, “Performance Analysis of VLSI Circuits in 45 nm Technology” — chapter in Advances in Decision Sciences, Image Processing, Security and Computer Vision (Learning and Analytics in Intelligent Systems, vol. 4 — Springer), 2020.
   DOI: 10.1007/978-3-030-24318-0_34
3. M. Dasharatha, B. Rajendra Naik, N. S. S. Reddy, Shoban Mude, “VLSI Design and Synthesis of Reduced Power and High Speed ALU Using Reversible Gates and Vedic Multiplier”— chapter in Advances in Decision Sciences, Image Processing, Security and Computer Vision (Springer), 2020.
   DOI: 10.1007/978-3-030-24318-0_33

MoUs Initiated:

- Nodal officer for MoU between Osmania University and Shibaura Institute of Technology, Tokyo, Japan for collaborative projects to enhance global learning and academic exchange (2023).
- Nodal officer for MoU between Osmania University and The Singareni Collieries Company Limited to sponsor construction of four classroom complex in the ECE Department, UCE(A) as part of CSR initiatives, in the larger interest of engineering education (2021).