With effect from academic year 2021-22

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Scheme of Instruction

and

Syllabus of

M.E. (E.C.E.)

EMBEDDED SYSTEMS AND VLSI DESIGN

Full Time & PTPG

AICTE Model Curriculum

2021-22

UNIVERSITY COLLEGE OF ENGINEERING
(Autonomous)
Osmania University
Hyderabad – 500 007, TS, INDIA

M.E. (ECE-Embedded Systems and VLSI design)

Type of course	Course Code	Course Name	Contact hours per week			Scheme of Examination		Credits
			L	T	P	CIE	SEE	
SEMESTER-I								
Core-I	EC401	Analog and Digital CMOS VLSI Design	3	0	0	30	70	3
Core-II	EC402	Microcontrollers and Programmable Digital Signal Processor	3	0	0	30	70	3
Programme Elective-I	EC111	Advanced Computer Architecture	3	0	0	30	70	3
	EC411	CPLD and FPGA Architectures						
Programme Elective-II	EC412	Satellite Navigation System	3	0	0	30	70	3
	EC413	System on Chip Design						
Audit Course -I	AC 031	English for Academic and Research Writing	2	0	0	30	70	0
	AC 032	Disaster Management						
	AC 033	Sanskrit for Technical Knowledge						
	AC 034	Value Education						
Lab-I	EC 451	Programmable Controllers and CMOS VLSI Design Laboratory	0	0	3	50	-	1.5
	EC 461	Seminar-I	0	0	3	50	-	1.5
MC	EC100	Research Methodology in ECE	3	0	0	30	70	3
TOTAL			**17**	**0**	**6**	**280**	**420**	**18**
SEMESTER-II								
Core-III	EC103	VLSI Design Verification and Testing	3	0	0	30	70	3
Core-IV	EC 403	Embedded Systems and Real Time Operating Systems	3	0	0	30	70	3
Programme Elective-III	EC 414	VLSI Physical Design	3	0	0	30	70	3
	EC 116	Internet of Things						
Programme Elective-IV	EC 415	VLSI Technology	3	0	0	30	70	3
	EC 416	VLSI Signal Processing						
Audit Course -II	AC 035	Stress Management by Yoga	2	0	0	30	70	0
	AC 036	Personality Development through life enlightenment skills						
	AC 037	Constitution of India						
	AC 038	Pedagogy Studies						
Lab-II	EC 452	VLSI Design Verification and RTOS Laboratory	0	0	3	50	-	1.5

	EC 462	Seminar-II	0	0	3	50	-	1.5
	EC 070	Mini Project	0	0	6	50	-	3
TOTAL			**14**	**0**	**12**	**300**	**350**	**18**
SEMESTER-III								
Programme Elective-V	EC119	Analog and Mixed Signal IC Design	3	0	0	30	70	3
	EC118	Low Power VLSI Design						
	EC 121	Applications of Nanotechnology						
Open Elective	OE 941	Business Analytics	3	0	0	30	70	3
	OE 942	Industrial Safety						
	OE 943	Operations Research						
	OE 944	Cost Management of Engineering Projects						
	OE 945	Composite Materials						
	OE 946	Waste to Energy						
	OE 947	Internet of Things						
	OE 948	Cyber Security						
Dissertation	EC481	Major project phase- I	0	0	20	100	-	10
TOTAL			**6**	**0**	**20**	**160**	**140**	**16**
SEMESTER-IV								
Dissertation	EC482	Major project phase- II	0	0	32	-	200	16
GRAND TOTAL								**68**

CIE: Continuous Internal Evaluation SEE: Semester End Examination

SEMESTER - 1

EC 401

ANALOG AND DIGITAL CMOS VLSI DESIGN

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.*
- *Connect the individual gates to form the building blocks of a system and using EDA tools like Cadence, Mentor Graphics and other open source software tools like Spice.*
- *Understand the advanced technologies and Passive and active current mirrors*

Outcomes: *At the end of this course, students will be able to:*

1. *Design MOS transistor circuits*
2. *Know the Physical design flow and different modelling design*
3. *Design sequential circuits at higher level*
4. *Design analog circuits like single stage and differential amplifiers*
5. *Analyze frequency response of active circuits*

UNIT – I

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, Delay, Wire delay models. Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model.

UNIT – II

Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, transmission gate logic.

UNIT – III

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, and Non-bistable sequential circuit.

Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, and TFET.

UNIT – IV

Single Stage Amplifier: CS stage with resistance load, Diode connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascode stage, Choice of device models.

Differential Amplifiers: Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT – V

Passive and active current mirrors: Basic current mirrors, Cascode mirrors, Active current mirrors.

References:

1. J P Rabaey, A P Chandrakasan, B Nikolic, *"Digital Integrated circuits: A design perspective"*, Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "*CMOS Circuit Design, Layout, and Simulation*", Wiley, 2nd Edition.
3. BehzadRazavi , "*Design of Analog CMOS Integrated Circuits",* TMH, 2007
4. Phillip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design"*, Oxford, 3rd Edition.
5. Kang, S. and Leblebici, Y., *"CMOS Digital Integrated Circuits, Analysis and Design*", TMH, 3rdEdition.
6. Pucknell, D.A. and Eshraghian, K., "*Basic VLSI Design*", PHI, 3rd Edition.

EC 402

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To understand the instructions and program the 8051*
- *To gain the knowledge of ARM cortex on Zynq for Embedded systems and on LPC 214xx microcontroller.*
- *To understand basic features of programmable DSP processor and to study instruction set and addressing modes of TMS 320C 54XX.*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand the architecture of a microcontroller to design applications using them.*
2. *Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.*
3. *Develop simple applications using LPC 214xx microcontroller.*
4. *Identify and characterize architecture of Programmable DSP Processors.*
5. *Develop small applications by utilizing the ARM processor core and DSP processor-based platform.*

UNIT – I

Microcontroller architecture: Review of 8051 architecture: 8051 registers, Memory organizations-program memory and data memory, internal RAM and bit addressable memory, special functions register. Interfacing 8051 with peripherals – LCD, Stepper motor, ADC, DAC, PWM, Relay.

UNIT – II

ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, ARM processor fundamentals,LPC 214x microcontrollerFeatures, architecture, Internal memory, system control, pin connect block, GPIOs, Timers, ADC, UART, CAN, I2C, Pulse Width Modulation, RTC, WDT.

UNIT – III

LPC 214x microcontroller Interfacing with real world: Basic Instructions and Assembly language programming- Arithmetic, Logical, and branching instructions, C-language programming for Interfacing with LCD display, Keypad and DC motors, serial programming.

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UNIT – IV

Programmable DSP Processors: Basic Architectural features, DSP Computational Building blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation unit, Programmability and Program execution, Speed Issues.

UNIT – V

Commercial Digital Signal-Processing Devices: Data addressing modes of TMS320C54xx Digital signal processors, Data Addressing modes of TMS320C54xx processors, Memory space of TMS32054xx processors, Program control, TMS320C54xx instructions and programming, On-chip peripherals, Interrupts of TMS320C54xx processors, pipeline operation of TMS320C54xx processors.

References:

1 Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin D.McKinlay, "*The 8051 Microcontroller and Embedded Systems using Assembly and C*", 2nd Edition, Pearson education, 2009.

2 Sloss Andrew N, Symes Dominic, Wright Chris, "*ARM System Developer's Guide: Designing and Optimizing"*, Morgan Kaufman Publication

3 User Manual of LPC214X Microcontroller

4 Avatar Singh and Srinivasan. S, *"Digital Signal Processing Implementations",* Thomson Books, Singapore, 2004.

5 Venkatramani B. and Bhaskar M *"Digital Signal Processors: Architecture, Programming and Applications"* , TMH , 2nd Edition

EC 111

ADVANCED COMPUTER ARCHITECTURE
(PROGRAM SPECIFIC ELECTIVE – I)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To Design Basic Data Path Unit (DPU) and Control Unit (CU) and to Familiarize with Parallel Processing Architectures*
- *To Develop OpenCL Programming Environment and developing Kernel Programming*
- *To Know Heterogeneous Architectures*

Outcomes: *At the end of this course, students will be able to:*

1. *To Realize Data Path Unit (DPU) and Control Unit (CU)*
2. *To Analyze the Performance of Multi-Core Architectures*
3. *To Demonstrate OpenCL Programs for real time applications*
4. *To Implement Kernels for Heterogeneous Architectures in OpenCL*
5. *To List and Describe the Challenges in Advanced Parallel Processing Architectures*

UNIT – I

Processor Design:

CPU Design– CPU Organization – Data Path Design: Fixed Point Booth's Multiplier, Restoring Division Unit and Non-Restoring Division Unit.
Memory Hierarchy **–** Virtual Memory – Cache Memory
Control Unit Design – Hardwired Control Unit Design of Basic CPU.
Case Studies:Verilog HDL Implementation of Booth's Multiplication, Restoring and Non-Restoring Division and Hardwired Control Unit Realization of Basic CPU

UNIT – II

Multi Core Architectures:

RISC, CISC, Flynn's Classification, Instruction Level Parallelism: Super Scalar, VLIW and EPIC architectures. Scalable, Multithreaded and Dataflow Architectures: Principles of Multithreading, Fine-Grain Multithreading, Scalable and Multithreaded Architectures and Dataflow and Hybrid Architectures.
*Case Studies:*Threads and OpenMP

UNIT – III

Accelerated Architectures:

GPU: nVidia and AMD Architecture – GPU memory and Scheduling, Parallel Programming Development and Environment: MPI – CUDA – OpenCL: Introduction, Platform and Devices, Execution Environment and Memory Model
Case Studies: OpenCL programming

UNIT – IV

Low Power Architectures: System on Chip Architectures – Raspberry-Pi, nVidia SoC – Basics of Kernels: Kernels, Work-items, Work-groups and Execution Domain, OpenCL Synchronization
Case Studies: Programming on Raspberry Pi.

UNIT – V

Advances in Parallel Processor Architectures:

Hybrid Architectures– Issues and Challenges in Heterogeneous Computing, Schedulers, Process Synchronization and Programming

Virtualization– Processor and Memory

*Case Studies:*Hybrid Programming using CPU and GPU

References:

1. Hayes John P, "*Computer Architecture and organization,"* 3rd edition, McGraw Hill Education, 1998.
2. William Stallings, *"Computer Organization and Architecture: Designing for Performance",* 8th edition, PHI, 2007.
3. Hwang and Naresh Jotwani, *"Advanced Computer Architecture: Parallelism, Scalability and Programmability*," McGraw Hill Education, 2017.
4. Benedict Gaster, Lee Howes, David R. Kaeli, Perhaad Mistry and Dana Schaa, *"Heterogeneous Computing with OpenCL,"* Morgan Kaufmann Publications, 2011.

EC411

CPLD AND FPGA ARCHITECTURE
(PROGRAM SPECIFIC ELECTIVE – I)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *Understand the basic operation of Programmable gate arrays*
- *Learn the architecture of various types of FPGAs/CPLD and design a digital circuit and implement it on an FPGA,*
- *Implemented the programming techniques used in FPGA design and Verification, testing FPGAs.*

Outcomes: *At the end of this course, students will be able to:*

1. *Evaluation of PLDs*
2. *Familiarity architecture of various types of FPGAs/CPLD.*
3. *Design a digital circuit and implement it using reconfigurable logic.*
4. *Design and develop IP cores and Prototypes in FPGA design.*
5. *Apply simulators and verify develop FPGA designs.*

UNIT – I

*Programmable Logic Devices:*Revision of basic Digital systems, PROM, PLA, PAL, Architecture of PAL's applications, programming technologies, programmable logic design methods and tools.

UNIT – II

CPLD's: complex programmable logic devices: logic block, I/O block, interconnect matrix, logic blocks and features of altera flex logic 10000 series CPLD‟s , max 7000 series CPLD‟s, AT & T– ORCA's (Optimized Reconfigurable Cell Array), cypres flash 370 device technology, lattice plsi's architectures.

UNIT – III

FPGAs: Field Programmable Gate Arrays: Logic blocks, routing architecture, Logic cells and features of commercially available FPGA‟s- XILINX XC4000, SPARTAN II, virtexII FPGA‟s, XILINX, Altera's FPGA, ACETEL Act1, Act2, Act3 FPGAS , AMD FPGA.

UNIT – IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement
Placement, simulated annealing.
Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays,Computing signal delay in RC tree networks.

UNIT – V

*FPGA implementation steps:*Synthesis and simulationprocess, verification: introduction, logic simulation, design validation, timing verification. Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, programmability failures, Case studies: programmable counter,ALU,Barrel shifter.

References:

1 P.K. Chan & S. Mourad, *"Digital Design Using Field Programmable Gate Array",* Pearson Education 2009.

2 S. Trimberger, Edr.,*"Field Programmable Gate Array Technology",* Kluwer Academic Publications, 1994.

3 J. Old Field, R. Dorf, *"Field Programmable Gate Arrays*", John Wiley & Sons, Newyork, 1995.

4 S. Brown, R. Francis, J. Rose, Z.Vransic, *"Field Programmable Gate array*", Kluwer Publn, 1992

5 *Manuals* from Xilinx, Altera, AMD, Actel.

EC 412

SATELLITE NAVIGATION SYSTEM
(PROGRAM SPECIFIC ELECTIVE – II)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To understand about the Satellite Subsystems, launch vehicles and Earth station*
- *To study about different types of receivers, coordinate systems and GNSS errors*
- *To analyze the significance of other GNSS constellations, SBAS and their applications.*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand the various principles related to Satellite communication systems.*
2. *Study the operation of GNSS, its signal structure and receiver types.*
3. *Estimate the various GNSS errors and understand the RINEX data format.*
4. *Compare the various features of other GNSS constellations, SBAS and GBAS*
5. *Analyze the applications of Satellite Navigation Systems.*

UNIT – I

*Review of Satellite communications:*Origin of Satellite Communication**,** basic principles and properties of Satellite communication, Spacecraft subsystems, Earth Stations: Functional block diagram and its operation, Merits and limitations of Large, Medium and Small Earth stations, Satellite launches: SLV, ASLV, PSLV and GSLV, Orbital effects on Satellite communication system performance.

UNIT – II

Basics of GNSS: Trilateration, Introduction and Heritage of NAVSTAR GPS, GPS Principle of operation, architecture, operating frequencies, advantages and limitations of GPS, orbits, GPS and UTC Time, GPS Signal structure, C/A and P-Code, ECEF and ECI coordinate systems and WGS 84, Operation of Generic GPS receiver functional block diagram, Types of GPS Receivers: Dual, Single frequency code, carrier smoothed, code & carrier receivers.

UNIT – III

*GNSS Errors:*Ionospheric error, Tropospheric error, Ephemeris error, Clock errors, Satellite and receiver instrumental biases, Multipath, Dilution of Precision, Spoofing and Anti-spoofing, GPS Modernization program, Objectives and important features, RINEX Navigation and Observation data formats.

UNIT – IV

*GNSS and Augmentation systems:*GLONASS, GALILEO, COMPASS, QZSS, IRNSS-Architecture, their operation, current status, Comparisons of all GNSS, Need for Satellite Based Augmentation and Local Area Augmentation Systems (SBAS and GBAS) and its operation, Advantages and limitations of SBAS and GBAS.

UNIT – V

GNSS Navigation Applications: Applications of GNSS to Land Vehicle Navigation and Tracking, Marine applications, Air Traffic Control, Surveying, Mapping and Geographical Information Systems, Military and Space, Recreation and Sports, Timing and Synchronization, Public related and Indoor navigation.

References:

1 B.HofmannWollenhof, H.Lichtenegger, and J.Collins, "*GPS Theory and Practice"*, Springer Wien, York, 2000.

2 Pratap Misra and Per Enge, *"Global Positioning System Signals, Measurements, and Performance,"* Ganga-Jamuna Press, Massachusetts, 2001.

3 Ahmed El-Rabbany, *"Introduction to GPS,"* Artech House, Boston, 2002.

4 Bradford W. Parkinson and James J. Spilker, "*Global Positioning System: Theory and Applications,"* Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.

5 Elliot D. Kaplan, *"Understanding GPS Principles and Applications"*, Artech House Boston, 1996.

EC 413

SYSTEM ON CHIP DESIGN
(PROGRAM SPECIFIC ELECTIVE – II)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To Understand the System Architecture and Processor Architecture, approach for a SOC Design and the concept of pipelining.*
- *To Learn about SOC external memory, Scratchpads and Cache memory and Multilevel Caches.*
- *To familiarize with on-chip memory concepts for SoC and to adopt the architectural support for operating systems.*

Outcomes: *At the end of this course, students will be able to:*

1. *Analyze the system and processor architecture approach for SoC design*
2. *Explore the concept of pipelining.*
3. *Understand the concept of memory interface and bus architecture for SoC design.*
4. *Analyze the performance metrics of on-chip memory.*
5. *Understand the architectural support for operating systems.*

UNIT – I

*Introduction to System on Chip:*System Architecture components of the system, hardware andSoftware, processor architecture, memory and addressing, system level interconnection, anApproach for SOC design, system architecture and complexity.
Processor design: Processor architecture and organization, processor design trade-offs, theReduced instruction set computer, the acron risc machine, architectural inheritance, the armProgrammers model, arm development tools.

UNIT – II

*Organization of an SoC:*3-stage pipeline arm organization, 5-stage pipeline arm organization, the arm coprocessor interface coprocessor instructions, data operations, data transfers, the thumb bit in the cpsr, the thumb programmer's model

UNIT – III

Architectural support for system development: The arm memory interface, the advanced micro controller bus architecture (amba), the arm reference peripheral specification, hardware system prototyping tools, the armulator, the jtag boundary scan test architecture embedded trace, signal processing support.

UNIT – IV

*Memory hierarchy:*Memory size and speed: memory cost, on chip memory, caches: processor
& memory speeds, unified & Harvard caches, cache performance metrics, the direct mappedCache the set-associative cache, the fully associative cache, write strategies cache design-an example.

UNIT – V

Architectural support for operating systems: An introduction to operating system, the armSystem control coprocessor, cp15 protection unit register, arm protection unit, cp15 mmuRegisters, arm mmu architecture, synchronization, context switching, input/ouput.

References:

1 Steve furber, *"arm system-on-chip architecture"*, second edition, pearson publications
2 Andrew n.sloss, domnic symes,chris wright, *"arm system developers guide"*,publicationsElsevier.

EC 100

RESEARCH METHODOLOGY IN ECE

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To know the motivation on research philosophy and processes in general.*
- *To be able to formulate the problem statement and prepare research plan for the problem under investigation through literature.*
- *To be able to apply various techniques for data analysis and patenting*

Outcomes:

1. *Students able to understand research methodology and problems*
2. *Able to define the techniques involved in defining problem*
3. *Able to Developing a Research plan and research set up*
4. *Able to analyze the collection of data and statistical analysis*
5. *Able to have knowledge on writing the report and patenting*

UNIT – I

Objectives and Types of research: Objectives and Motivation of research- types of research-Research approaches – Significance of Research-Research Methods versus Methodology-Research and Scientific method- Importance of research methodology – Research process-criteria of good research- Problems encountered by Researchers in India-benefits to society in general.

UNIT – II

Research formulation: Defining and formulating the research problem, selecting the problem, importance of literature review in define a problem, literature review, primary and secondary sources, reviews, monograms, patents, research data bases web as a source, identifying gap areas from literature review and research data bases, devilment of working hypothesis

UNIT – III

Research Design and methods: Meaning of research design - need of research design-features of a good design- important concepts relating to research design- different research designs- Basic Principles of experimental designs- Developing a Research plan-Exploration, descriptions diagnosis and experiment

UNIT – IV

Execution of the research and data collection: Aspect of method validation, observation and collection of data, methods of data collection, sampling methods, data processing and analysis, strategies and tool, data analysis with statistical packages (sigma STAT, SPSS for student test t-test, ANOVA, etc.) hypothesis testing, generalization and interpretation.

UNIT – V

Reporting and thesis writing: Structure and components of scientific reports, types of report, technical report and thesis. Thesis writing-different steps and software tools (word processing) in the design and preparation of thesis, layout, structure (chapter plan) and language of typical reports, illustrations and tables, bibliography, referencing and footnotes. Use of visual aids.

Patenting: The Basics of the Patent System, Patent Law, How to Read a Patent, Protecting Invention and Planning Patent Filing, Preparing Patent Application

References:

1 C.R.Kothari, "*Research methodology, Methods & technique*", New age international publishers,2004.

2 R.Ganesan, "*Research Methodology for Engineers*", MJP Publishers: Chennai, 2011.

3 P.Ramdass and A.Wilson Aruni, *"Research and Writing across the disciplines",* MJP Publishers, Chennai 2009

4 Matthew Y Ma,"Fundamentals of Patenting and Licensing for Scientists and Engineers" 2nd Edition 2015

AC 031

ENGLISH FOR ACADEMIC AND RESEARCH WRITING
(AUDIT COURSE-I)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives: *To expose the students to...*

- *Features of Academic writing; different kinds of Academic writing*
- *Some academic writing skills; the research process; the structure of a research document*

Outcomes: *At the end of this course, students will be able to:*

1. *Academic writing features; Academic writing kinds; Important academic writing skills*
2. *The process of research; general research document structure*

UNIT – I
Features of Academic Writing
Language: Clear, Correct, Concise, Inclusive; **Tone**: Formal, Objective, Cautious; **Style**: Appropriate, Accurate, Organized; **Ethics**: Honesty, Integrity, Responsibility, Accountability

UNIT – II
Kinds of Academic Writing: Essays, Reports, Reviews, Abstracts, Proposals

UNIT – III
Academic Writing Skills
Paraphrasing; Summarizing; Quoting; Rewriting; Expansion

UNIT – IV
Research Process
Selection of Topic, Formulation of Hypothesis, Collection of Data, Analysis of Data, Interpretation of Data, Presentation of Data

UNIT – V
Structure of a Research Document
Title, Abstract, Introduction, Literature Survey, Methodology, Discussion, Findings/Results, Conclusion, Documenting Sources (IEEE style)

References:

1 Bailey, S. (2014). *Academic writing: A handbook for international students*. Routledge.
2 Gillett, A., Hammond, A., &Martala, M. (2009). *Inside track: Successful academic writing*. Essex: Pearson Education Limited.
3 Griffin, G. (2006). *Research methods for English studies*. Edinburgh: Edinburgh University Press.
4 Silyn-Roberts, Heather. (2013). *Writing for Science and Engineering: Papers, Presentations and Reports* (2nd Ed.). Elsevier.
5 Lipson, Charles (2011). *Cite right: A quick guide to citation styles; MLA, APA, Chicago, the sciences, professions, and more* (2nd Ed.). Chicago [u.a.]: University of Chicago Press.

AC 032

DISASTER MANAGEMENT
(AUDIT COURSE-I)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *To impart knowledge in students about the nature, causes, consequences and mitigation measures of the various natural disasters*
- *To enable the students to understand risks, vulnerabilities and human errors associated with human induced disasters*
- *To enable the students to understand and assimilate the impacts of any disaster on the affected area depending on its position/ location, environmental conditions, demographic, etc.*

Outcomes: *At the end of this course, students will be able to**:***

1. *Learn to demonstrate a critical understanding of key concepts in disaster risk reduction*
2. *Humanitarian response*
3. *Critically evaluate disaster risk reduction and humanitarian response policy and Practice from multiple perspectives.*
4. *Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.*
5. *Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in**.***

UNIT – I

Introduction: Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT – II

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem.
Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT – III

*Disasters Prone Areas in India:*Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT – IV

Disaster Preparedness and Management
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluationof Risk: Application of Remote Sensing, Data From Meteorological and OtherAgencies, Media Reports: Governmental and Community Preparedness.

UNIT – V

Risk Assessment

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and NationalDisaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT – VI

Disaster Mitigation

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends inMitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

References:

1 R. Nishith, Singh AK, *"Disaster Management in India: Perspectives, issues and strategies"*, New Royal Book Company.

2 Sahni, Pardeep (Eds.), *"Disaster Mitigation Experiences and Reflections"*, PHI, New Delhi.

3 Goel S. L., *"Disaster Administration and Management Text and Case Studies",* Deep & Deep Publication Pvt. Ltd., New Delhi.

AC 033

SANSKRIT FOR TECHNICAL KNOWLEDGE
(AUDIT COURSE-I)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *To get a working knowledge in illustrious Sanskrit, the scientific language in the world*
- *Learning of Sanskrit to improve brain functioning*
- *Learning of Sanskrit to develop the logic in mathematics, science & other subjects*
- *enhancing the memory power*
- *The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature*

Outcomes: *At the end of this course, students will be able to:*

1. *Understanding basic Sanskrit language*
2. *Ancient Sanskrit literature about science & technology can be understood*
3. *Being a logical language will help to develop logic in students*

UNIT – I

- Alphabets in Sanskrit,
- Past/Present/Future Tense,
- Simple Sentences

UNIT – II

- Order
- Introduction of roots
- Technical information about Sanskrit Literature

UNIT – III

- Technical concepts of Engineering-Electrical, Mechanical,Architecture, Mathematics

References:

1 "*Abhyaspustakam*" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2 "*Teach Yourself Sanskrit*" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya SanskritSansthanam, New Delhi Publication
3 "*India's Glorious Scientific Tradition*" Suresh Soni, Ocean books (P) Ltd., New Delhi.

AC 034

VALUE EDUCATION
(AUDIT COURSE-I)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives: *Students will be able to*

- *Understand value of education and self- development*
- *Imbibe good values in students*
- *Let the should know about the importance of character*

Outcomes: *At the end of this course, students will be able to:*

1. *Knowledge of self-development*
2. *Learn the importance of Human values*
3. *Developing the overall personality*

UNIT – I

Values and self-development –Social values and individualattitudes. Work ethics, Indian vision of humanism.Moral and non- moral valuation. Standards and principles.Value judgements

UNIT – II

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence,Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism.Love for nature,Discipline

UNIT – III

Personality and Behavior Development - Soul and Scientificattitude. Positive Thinking. Integrity and discipline.Punctuality, Love and Kindness.Avoid fault Thinking.Free from anger, Dignity of labour. Universal brotherhood and religious tolerance.True friendship.Happiness Vs suffering, love for truth.Aware of self-destructive habits. Association and Cooperation.

UNIT – IV

Doing best for saving nature, Character and Competence –Holy books vs Blind faith, Self-management and Good health.Science of reincarnation.Equality, Nonviolence,Humility, Role of Women.All religions and same message.Mind your Mind, Self-control.Honesty, Studying effectively

References:

1 Chakroborty, S.K., *"Values & Ethics for organizations Theory and practice*", Oxford University Press, New Delhi, 1998.

EC 451

PROGRAMMABLE CONTROLLERS AND CMOS VLSI DESIGN LABORATORY

Instruction: 3 periods per week *Duration of SEE: --*
CIE: 50 marks *SEE: --*
Credits: 1.5

Objectives:

- *To create, develop, apply, and disseminate knowledge within the microcontroller-based application development environment.*
- *To understand interfacing of basic peripherals with microcontrollers & ARM processors and to Know Basics of System Verilog and test coverage in System Verilog.*
- *To Familiarize with Object Oriented Programming and System Verilog and Explore Randomization and Threads in System Verilog.*

Outcomes:

1. *To write an assembly language programming to perform different arithmetic, logic, looping and branching operations on ARM processors.*
2. *To interface different programmable devices to 8051 & ARM Microcontrollers and control them by writing assembly language/embedded C programming.*
3. *To Realize and Verify Combinational and Sequential Circuits in Verilog HDL*
4. *To Create Object Oriented Programming Environment.*
5. *To Propose Efficient Testable Digital Systems in System Verilog.*

Cycle I

Part A: Interfacing Programs Using KEIL µvision Software on 8051 µc Development Board.

1. Assembly Language Program to Interface 7 – Segment Display to 8051 Microcontroller.
2. Assembly Language Program to display message in a 2 line x 16 characters LCD display.
3. Assembly Language program for interfacing Keypad to 8051 Microcontroller.
4. Assembly Language program for interfacing DAC to generate different waveforms.
5. Assembly Language program for interfacing stepper motor and to control it.

Part B: Implement the following Programs on ARM Processor.

1. Simple Assembly Program for
    a. Addition | Subtraction | Multiplication | Division
    b. Operating Modes, System Calls and Interrupts
    c. Loops, Branches
2. Assembly programs to configure and control General Purpose Input-Output (GPIO) pins.
3. Programs to interface 8-Bit LED and control them.
4. Interfacing real time clock and serial port.
5. Keyboard (4X4 matrix) Interface to ARM Processor.
6. LCD Interface to ARM Processor.
7. Interfacing EPROM and interrupt programming in ARM Processor.
8. Stepper motor Interface to ARM Processor
9. Assembly program for Mailbox.
10. Generation of PWM Signal

Cycle II:

Experiments:

1. Design of CMOS Inverter &two input NAND Gate.
2. Design of Half Adder using NAND Gates
3. Design a Full Adder using transmission gate logic.
4. Design a Schmitt trigger circuit using CMOS logic
5. Design of 4-bit Adder using Full Adder.
6. Design a 4bit barrel shifter
7. Design of 4-bit thermometer to Binary Code converter.
8. Design and draw the layout of above Digital Circuits.
9. Analyze a two-level RC interconnect circuit for a step input
10. Analyze a tree level inductive interconnect model circuit
11. Design a common source amplifier and find its characteristics.
12. Design a current mirror circuits using MOSFET.

EC 461

SEMINAR – I

Instruction: 3 periods per week *Duration of SEE: --*
CIE: 50 marks *SEE: --*
Credits: 1.5

Outcomes: *At the end of this course, students will be able to:*

1. *Develop the habit of referring the journals for literature review.*
2. *Understand the gist of the research paper.*
3. *Identify the potential for further scope.*
4. *Present the work in an efficient manner.*
5. *Write the documentation in standard format.*

Seminar topics may be chosen by the students with advice from the faculty members and the student shall read further relevant articles in the domain.

The seminar must be clearly structured and the power point presentation shall include following aspects:

1. Introduction to the field
2. Literature survey
3. Consolidation of available information
4. Summary and Conclusions
5. References

Each student is required to:

1. Deliver the seminar for a maximum duration of 30 minutes, where the presentation should be for 20 minutes in PowerPoint, followed by Question and Answers session for 10 minutes.
2. Submit the detailed report of the seminar in spiral bound in a précised format as suggested by the Department.

Guidelines for awarding marks		
S. No.	**Description**	**Max. Marks**
1	Contents and relevance	10
2	Presentation skills	10
3	Preparation of PPT slides	05
4	Questions and answers	05
5	Report in a prescribed format	20

Note:

1. The seminar presentation should be a gist of at least five research papers from **Peer-reviewed** or **UGC recognised** journals.
2. **The seminar report should be in the following order:** Background of work, literature review, techniques used, prospective deliverables, discussion on results, conclusions, critical appraisal and reference.
3. At least two faculty members will be associated with the seminar presentation to evaluate and award marks.
4. Attendance of all the students for weekly seminar presentations is compulsory. If the student fails to secure minimum attendance as per O.U. rules, the marks awarded in the seminar presentation shall remain void.

SEMESTER - II

EC 103

VLSI DESIGN VERIFICATION AND TESTING

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To Develop Structural, Dataflow and Behavioral Modeling of Verilog HDL.*
- *To Know Basics of System Verilog and Familiarize with Object Oriented Programming*
- *To Explore Randomization and Threads in System Verilog an also, to Know Test Coverage in System Verilog*

Outcomes: *At the end of this course, students will be able to:*

1. *To Realize and Verify Combinational and Sequential Circuits in Verilog HDL*
2. *To Construct User Defined Data Types in System Verilog*
3. *To Create Object Oriented Programming Environment*
4. *To Demonstrate Randomization and Coverage Concepts of System Verilog*
5. *To Propose Efficient Testable Digital Systems in System Verilog*

UNIT – I

Introduction to Verilog

Verilog Basics: Modules and Ports, Structural, Data Flow, Behavioral and switch level Modeling, Tasks and Functions, Logic Synthesis, Timing Delays.

Static timing analysis: Setup time & hold time violations, clock skew.

UNIT – II

Introduction to Verification

Verification guidelines: Verification Process, Test bench creation, Significance of Verification, Verilog for verification.

Introduction to System Verilog: Advantages over Verilog, Methodology, Randomization basics, Coverage basics

Data Types: Built-in data types, Fixed and dynamic Arrays, Queues, Associative Arrays, Enumerated data types, Procedural statements, Time values.

UNIT – III

Introduction to Object Oriented Programming (OOP): Communication between the Test bench and DUT, Interface Construct, Stimulus Timing, Interface Driving and Sampling, Programming block basics, System Verilog assertions.

OOP: Object Oriented Programming significance and advantages, classes, objects, object handles, methods, Static and Global Variables, using one class inside another class, Dynamic objects, copying objects, Public Vs Local and Building a test bench, Tasks and Functions.

UNIT – IV

Verification using System Verilog

Randomization: Significance, randomization in system Verilog, Constraint randomization, atomic stimulus generation, random number generation, constraint tips and techniques.

Threads: Threads, inter process communication, Events, Semaphores, Mailboxes virtual methods, Copying an Object, Inheritance, Abstract Classes and Pure Virtual Methods. Case

study using Verification Machine.

UNIT – V

Advanced System Verilog: Callbacks, Parameterized Classes, Static and Singleton Classes
Coverage: Introduction, Coverage Types, Functional Coverage Strategies, cover group, defining cover groups in classes, Data sampling, coverage points, Coverage methods, Cross coverage, Case study using Universal Verification Machine (UVM).

References:

1 Ming-Bo Lin., "*Digital System Designs and Practices Using Verilog HDL and FPGAs"*, Wiley India, 2008.
2 Samir Palnitkar, "*Verilog HDL: A Guide to Digital Design and Synthesis"*, Pearson Education, 2005.
3 Christ Spear and Greg Tumbush, "*System Verilog for Verification"*, 3rd ed., Springer, 2012.

EC 403

EMBEDDED SYSTEMS AND REAL TIME OPERATING SYSTEMS

Instruction 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To gain Knowledge to design Embedded Systems and tool chain for embedded systems*
- *To understand the importance of all Real Time Operating Systems and RTOS in building real time systems*
- *To get familiar with the standards like POSIX.*

Outcomes: *At the end of this course, students will be able to:*

1. *Design an Embedded system.*
2. *Use embedded software tools for designing embedded system applications.*
3. *Understand compatibility of RTOS with hardware targets.*
4. *Apply their understanding in building real time systems.*
5. *Able to design an embedded system with RTOS.*

UNIT – I

*Introduction to Embedded Systems and design life cycle:*Introduction to embedded systems, Embedded design life cycle, Product Specification, Hardware/Software Partitioning, Iteration and Implementation, Detailed Hardware and Software Design, Hardware/Software Integration, Product Testing and Release, Maintaining and Upgrading Existing Products.

UNIT – II

*A Basic Toolset:*Host-Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer, Bullet -Proof Run Control, Real-Time Trace, Hardware Breakpoints, Overlay Memory.

UNIT – III

Embedded Operating Systems: Concepts, Differences between Traditional OS and RTOS. Realtime System Concepts, Hard versus Soft Real-time systems – examples, Jobs & Processors, Hard and Soft timing, constraints, Hard Real-time systems, Soft Real-time systems. Classical Uniprocessor Scheduling Algorithms – RMS, Preemptive EDF, Allowing for Preemptive and Exclusion Condition.

UNIT – IV

Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability. Tasks and Task States, Tasks and Data, Semaphores and Shared Data, Message Queues, MailBoxes and Pipes, Timer Functions, Events, Memory Managements, Interrupt Routines in RTOS Environment.

UNIT – V

Commercial RTOS: VxWorks, μC/OS-II and RT Linux for Embedded Applications, Case Studies of Embedded Systems.

References:

1 Arnold Berger, *"Embedded Systems Design*", First South asian edition
2 David E Simon, *"An Embedded Software primer",* Low Price Edition, Pearson Education.
3 Betcnhof, D.R., *"Programming with POSIX threads",* Addison - Wesley Longman, 1997.
4 Wind River Systems, "*VxWorks Programmers Guide",* Wind River Systems Inc.1997.
5 Jean.J.Labrosse, "*MicroC/OS-II*", The CMP Books.
6 Jane W.S.Liu, *"Real Time Systems*", Pearson Education, Asia, 2001

EC 414

VLSI PHYSICIAL DESIGN
(PROGRAM SPECIFIC ELECTIVE – III)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *Draw the structure of passive active components*
- *Know the concepts of physical design and understand the layouts and stick diagrams of complex circuits*
- *Understand the system level physical design and floor planning and hands-on experience on CAD tools*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand the basic theory of BJT MOS transistors*
2. *Understand the basic concepts of physical design, layouts of BJT, MOS transistors and interconnect issues*
3. *Students are able to slove the performance issues in circuit layout*
4. *Able to analyze physical design problems and employ for partitioning, floor planning, placement and routing*
5. *Students are able to analyze circuits using both analytical and CAD tools*

UNIT – I

Scope of physical design, Components of VLSI, Various layers of VLSI, Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

UNIT – II

Basic concepts of Physical Design, layout of basic structures wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Mask overlays for different structures.Parasitics, latch up and its prevention. Device matching and common centroid techniques foranalog circuits.

UNIT – III

Design rules, fabrication errors, alignment sequence and alignment inaccuracies, processvariations and process deltas, drawn and actual dimensions and their effect on design rules–scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT – IV

Cell concepts, cell-based layout design, Weinberger image array, physical design of logic gates –NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, inter connect delay modelling, floor planning, routing and clock distribution.

UNIT – V

CAD Tools: Layout editors, Design rule checkers, circuit extractors, Hierarchical circuit extractors, Automatic layout tools, modelling and extraction of circuit parameters from physical layout. Input-Output Interfacing: Power Supply, Bonding pad, Pad Ring, Input structures, Digital output structures, Low Voltage Differential swing, Power clamp,

Core/Pad Limitation, Signal Propagation between Integrated Circuits.

References:

1. John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", John Wiley & sons, Inc.2012.
2. Wayne Wolf, *"Modern VLSI Design (System-on-Chip)",* Pearson Education, 3rd Edition 2005.
3. R. Jacob Baker; Harry W.Li., David E. Boyce, *"CMOS Circuit Design, Layout and Simulation",* IEEE Press, Prentice Hall of India.
4. Etienne Sicard Sonia Delmas Bendhia "*Advanced CMOS Cell Design"* Tata McGraw Hill First Edition 2007.
5. Preas, M. Lorenzatti, *"Physical Design and Automation of VLSI Systems",* the Benjamin
   Cummins Publishers, (1998).

EC 116

INTERNET OF THINGS
(PROGRAM SPECIFIC ELECTIVE – III)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To understand Smart Objects and IoT Architectures and learn about various IOT-related protocols*
- *To build simple IoT Systems using Arduino and Raspberry Pi*
- *To understand data analytics, cloud in the context of IoT and to develop IoT infrastructure for popular applications*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand the concepts of Internet of Things*
2. *Analyze basic protocols in wireless sensor network*
3. *Design IoT applications in different domain and be able to analyze their performance*
4. *Implement basic IoT applications on embedded platform*
5. *Understand the concepts of industrial applications*

UNIT – I

Fundamentals of IoT: Evolution of Internet of Things - Enabling Technologies – IoT Architectures: oneM2M, IoT World Forum (IoTWF) and Alternative IoT models – Simplified IoT Architecture and Core IoT Functional Stack -– Fog, Edge and Cloud in IoT – Functional blocks of an IoT ecosystem – Sensors, Actuators, Smart Objects and Connecting Smart Objects.

UNIT – II

IoT Protocols IoT access technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and LoRaWAN – Network Layer: IP versions, Constrained Nodes and Constrained Networks – Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks – Application Transport Methods: Supervisory Control and Data Acquisition – Application Layer Protocols: CoAP and MQTT.

UNIT – III

*Design and development design methodology***:** Embedded computing logic - Microcontroller, System on Chips - IoT system building blocks - Arduino - Board details, IDE programming - Raspberry Pi - Interfaces and Raspberry Pi with Python Programming.

UNIT – IV

Data analytics and supporting services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest – Role of Machine Learning – No SQL Databases – Hadoop Ecosystem – Apache Kafka, Apache Spark – Edge Streaming Analytics and Network Analytics – Xively Cloud for IoT, Python Web Application Framework – Django – AWS for IoT – System Management with NETCONF-YANG Developing.

UNIT – V

*Case studies/industrial applications***:** Manufacturing - Converged Plantwide Ethernet Model (CPwE) – Power Utility Industry – GridBlocks Reference Model - Smart and Connected Cities: Layered architecture, Smart Lighting, Smart Parking Architecture and Smart Traffic Control.

References:

1 David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, *"IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things*", Cisco Press, 2017

2 Vijay Madisetti, Arshdeep Bahga, *"Internet of Things: A Hands-On Approach*"

EC 415

VLSI TECHNOLOGY
(PROGRAM SPECIFIC ELECTIVE – IV)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To understand about the review of history of VLSI Technology progress.*
- *To analyze the process of realization of BJT and FET on an IC.*
- *To gain the knowledge related to Silicon Wafer Preparation and its various processes*

Outcomes: *At the end of this course, students will be able to:*

1. *Learn about the history of VLSI Technology progress since its inception*
2. *Understand the process realization of BJT on an IC.*
3. *Gain knowledge related realization of BJT on an IC.*
4. *Understand the process related to realization of FET on an IC.*
5. *Gain knowledge related to Ion implantation, Diffusion and Packaging processes*

UNIT – I

Introduction – Integrated Circuits Review of history of VLSI technology progress–. Electronic Functions –Components – Analog and Digital ICs. Basic Devices in ICs – Structures, Resistors – Capacitors – Inductors. Diodes – Bipolar Junction Transistors – Field Effect Transistors, Isolation techniques in MOS and bipolar Technologies.

UNIT – II

Monolithic ICs – Silicon as the Base Material and its advantages, Crystal Structure of Si , various Layers of ICs – Substrate – Active Layer -Oxide/Nitride Layers – Metal/Poly Silicon Layers – Functions of each of the layers. Process flow for Realization of Devices, Description of Process Flow for Typical Devices viz., FET and BJT**.**

UNIT – III

Silicon Wafer Preparation – Electronic Grade Silicon – CZ and FZ Methods of Single Crystal Growth – Silicon Shaping – Prefabrication Processes. Epitaxy: Growth Dynamics – Process Steps, Vapor phase, Solid phase and Molecular Beam Epitaxial Processes, Oxide Growth: Structure of SiO2, Growth Mechanism and Dynamics –Oxide Growth by Thermal method.

UNIT – IV

Deposition techniques Chemical Vapor Deposition (CVD), PVD thermal evaporation, Lithography: Steps involved in Photolithography – Quality of the Pattern – photo resists and their Characteristics, X-ray – Electron Beam Lithography. Etching: Chemical, Electro Chemical – Plasma (Dry Etching) Reactive Plasma Etching.

UNIT – V

Ion implantation: Range and Penetration Depth – Damage and Annealing – Ion Implantation machine. Diffusion: Constant and Infinite Source Diffusions – Diffusion Profiles – Diffusion Systems – Multiple Diffusions and Junction Formations, Clean rooms.

References:

1 .M. Sze., "*VLSI Technology",* Mc Grawhill International Editions.
2 Y Chang and S.M. Sze, "*VLSI Technology",* TataMcGraw-Hill Companies Inc.
3 D.Plummer,M.D.Deal and P.B.Griffin, *"The Silicon VLSI Technology Fundamentals, Practice and modeling"*, Pearson Education 2009
4 tephen A, Campbell and Elliot D. Kaplan, *"Understanding GPS Principles and Applications"*, Artech House Boston, 1996. The Science and Engineering of Microelectronic Fabrication, Oxford 20015

EC 416

VLSI SIGNAL PROCESSING
(PROGRAM SPECIFIC ELECTIVE - IV)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To enable the students to learn about the concept of pipelining and parallel processing in VLSI and the students to identify applications for unfolding algorithm To Design and Analyze Two-Stage Opamp*
- *To make the students to understand the analysis of VLSI system with high speed and low power and equip the students with knowledge of Systolic Design for Space Representations containing Delays*
- *To make the students to understand the concept of Power Reduction and Estimation techniques in VLSI signal processing*

Outcomes: *At the end of this course, students will be able to:*

1. *Explain parallel and pipelining processing techniques*
2. *Identify applications for unfolding algorithm*
3. *Analyze Systolic Design for Space Representations containing Delays.*
4. *Explain Cook-Toom Algorithm, Fast Convolution algorithm by Inspection method*
5. *Analyze Power Reduction techniques and Power Estimation techniques.*

UNIT – I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power, Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT – II

Folding and Unfolding, Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems, Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT – III

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT – IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT – V

Low Power Design: Scaling Vs Power Consumption–Power Analysis, Power Reduction techniques – Power Estimation Approaches, Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

References:

1. Keshab K. Parthi, *"VLSI Digital Signal Processing- System Design and Implementation"*, 1998, Wiley Inter Science.
2. Kung S. Y, H. J. While House, T. Kailath, *"VLSI and Modern Signal processing",* 1985, Prentice Hall.
3. Jose E. France, YannisTsividis, *"Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing",* 1994, Prentice Hall.
4. Medisetti V. K, *"VLSI Digital Signal Processing*", IEEE Press (NY), USA, 1995.

AC 035

STRESS MANAGEMENT BY YOGA
(AUDIT COURSE –II)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *To achieve overall health of body and mind.*
- *To overcome stress.*

Outcomes: *At the end of this course, students will be able to:*

1. *Develop healthy mind in a healthy body thus improving social health also*
2. *Improve efficiency.*

UNIT – I

Introduction: Definition of **Stress** – Types of stress: Acute and chronic - Stressors – Definition of **Yoga** from various sources – Types of yoga – Karma yoga, Gnana yoga, Bhakti yoga and Raja yoga – Concept of Bhagavad Geeta - Yoga versus exercise –Basics of Physiology and Psycholoy – Brain and its parts – CNS and PNS – HPA axis – Sympethetic and Para sympethetic nervous systems – Fight and Flight mechanism - Relationship between stress and yoga.

UNIT – II

Ashtanga Yoga: Do`s and Don'ts in life: i) **Yam** - Ahinsa, satya, astheya, bramhacharya and aparigraha ii) **Niyam** -Shaucha, santosh, tapa, swadhyay, ishwarpranidhan -iii) **Asana** iv) **Pranayama** v) **Prathyahara** vi) **Dharana** vii) **Dhyana** viii) **Samadhi** – Illustrations of eight steps of Ashtanga yoga.

UNIT – III

*Asana and Stress:*Definition of Asana from Pathanjali – Origin of various names of asanas - Various yog poses and their benefits for mind & body – Sequence of performing asanas: Standing, sitting, lying down on stomach, lying down on back and inverted postures – Activation of Annamaya kosha – Effect on various chakras, systems and glands thereby controlling the stress levels through the practice of asanas

UNIT – IV

*Pranayama and Stress:*Definition of pranayama from Shankaracharya - Regularization of breathing techniques and its effects - Types of pranayama – Heat generating and cold generating techniques – Pranayama versus chakras and systems – Breathing techniques versus seasons - Anger and breathing rate – Activation of pranamaya kosha – Pranayama as the bridge between mind and body – Stress control through pranayama.

UNIT – V

*Dhyana and Stress:*Distinction between Dhyana and Dharana– Preparation for Dhyana through prathyahara and dharana – Activation of Vignanamaya kosha – Types of mind: conscious, superconscious and subconscious – Activation of manomaya kosha through Dhyana – Silencing the mind thereby controlling the stress levels

References:

1 '*Yogic Asanas for Group Tarining-Part-I*' : Janardan Swami Yogabhyasi Mandal, Nagpur
2 "*Rajayoga or conquering the Internal Nature*" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata
3 Light on yoga by BKS Iyengar
4 "*The search for happiness and bliss*" by Swami Sarvapriyananda on you tube – https://youtu.be/xfywJTPkw7Y
5 "*Mastering the mind*" by Swamini Vimalananda on you tube - https://youtu.be/EXniWH9DMF8

AC 036

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS (AUDIT COURSE –II)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *To learn to achieve the highest goal happily*
- *To become a person with stable mind, pleasing personality and determination*
- *To awaken wisdom in students*

Outcomes: *At the end of this course, students will be able to:*

1. *Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life.*
2. *The person who has studied Geeta will lead the nation and mankind to peace and prosperity*
3. *Study of Neetishatakam will help in developing versatile personality of students.*

UNIT – I

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT – II

- Approach to day to day work and duties.
- Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT – III

- Statements of basic knowledge.
- Shrimad Bhagwad Geeta : Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta : Chapter2-Verses 17,Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

References:

1 Swami Swarupananda Advaita Ashram "*Srimad Bhagavad Gita",* (Publication Department), Kolkata

2 P.Gopinath, *"Bhartrihari's Three Satakam (Niti-sringar-vairagya*)", Rashtriya Sanskrit Sansthanam, New Delhi

AC 037

CONSTITUTION OF INDIA
(AUDIT COURSE –II)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective*
- *To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.*
- *To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.*

Outcomes: *At the end of this course, students will be able to:*

1. *Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.*
2. *Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India*
3. *Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.*
4. *Discuss the passage of the Hindu Code Bill of 1956.*

UNIT – I

History of Making of the Indian Constitution: History, Drafting Committee, (Composition & Working)

UNIT – II

Philosophy of the Indian Constitution: Preamble and Salient Features

UNIT – III

• **Contours of Constitutional Rights & Duties:**
  • Fundamental Rights
  • Right to Equality
  • Right to Freedom
  • Right against Exploitation
  • Right to Freedom of Religion
  • Cultural and Educational Rights
  • Right to Constitutional Remedies
  • Directive Principles of State Policy
  • Fundamental Duties.

UNIT – IV

• Organs of Governance:
  • Parliament
  • Composition
  • Qualifications and Disqualifications

- Powers and Functions
- Executive
- President
- Governor
- Council of Ministers
- Judiciary, Appointment and Transfer of Judges, Qualifications
- Powers and Functions

UNIT – V

• Local Administration:
- District's Administration head: Role and Importance,
- Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation.
- Pachayati raj: Introduction, PRI: ZilaPachayat.
- Elected officials and their roles, CEO ZilaPachayat: Position and role.
- Block level: Organizational Hierarchy (Different departments),
- Village level: Role of Elected and Appointed officials,
- Importance of grass root democracy

UNIT-VI

- **Election Commission:**
- Election Commission: Role and Functioning.
- Chief Election Commissioner and Election Commissioners.
- State Election Commission: Role and Functioning.
- Institute and Bodies for the welfare of SC/ST/OBC and women.

References:

1. *"The Constitution of India",* 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, *"Dr. B. R. Ambedkar framing of Indian Constitution",* 1st Edition, 2015.
3. M. P. Jain, "*Indian Constitution Law",* 7th Edn. Lexis Nexis, 2014.
4. D.D. Basu, *"Introduction to the Constitution of India",* Lexis Nexis, 2015.

AC 038

PEDAGOGY STUDIES
(AUDIT COURSE –II)

Instruction: 2 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 00

Objectives:

- *Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.*
- *Identify critical evidence gaps to guide the development.*

Outcomes: *At the end of this course, students will be able to:*

1. *What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?*
2. *What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?*
3. *How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?*

UNIT – I

*Introduction and Methodology:*Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions, Overview of methodology and Searching.

UNIT – II

*Thematic Overview:*Pedagogical practices followed by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education

UNIT – III

*Evidence on the Effectiveness of Pedagogical Practices***:** Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and Practicum) and the school curriculum and guidance material best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches – Teachers attitudes and beliefs and pedagogic strategies.

UNIT – IV

*Professional Development:*alignment with classroom practices and follow up support - Support from the head teacher and the community – Curriculum and assessment - Barriers to learning: Limited resources and large class sizes.

UNIT – V

*Research Gaps and Future Directions:*Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment – Dissemination and research impact.

References:

1 Ackers J, Hardman F, *"Classroom Interaction in Kenyan Primary Schools, Compare*", 31 (2): 245 – 261, 2001.

2 Agarwal M, *"Curricular Reform in Schools: The importance of evaluation*", Journal of Curriculum Studies, 36 (3): 361 – 379, 2004.

3 Akyeampong K, "*Teacher Training in Ghana – does it count? Multisite teacher education research project (MUSTER)",* Country Report 1. London: DFID, 2003.

4 Akyeampong K, Lussier K, Pryor J, Westbrook J, *"Improving teaching and learning of Basic Maths and Reading in Africa: Does teacher Preparation count?"*International Journal Educational Development, 33 (3): 272- 282, 2013.

5 Alexander R J, *"Culture and Pedagogy: International Comparisons in Primary Education",* Oxford and Boston: Blackwell, 2001.

6 Chavan M, Read India: *"A mass scale, rapid, learning to read campaign",* 2003

7 www.pratham.org/images/resource%20working%20paper%202.pdf.

EC 452

VLSI DESIGN, VERIFICATION AND RTOS LABORATORY

Instruction: 3 periods per week *Duration of SEE: --*
CIE: 50 marks *SEE: --*
Credits: 1.5

Objectives:

- *To Develop Structural, Dataflow and Behavioral Modeling of Verilog HDL.*
- *To Know Basics of System Verilog and to Familiarize with Object Oriented Programming*
- *To Explore Randomization and Threads in System Verilog and to Know Test Coverage in System Verilog*

Outcomes: *At the end of this course, students will be able to:*

1. *To realize and verify combinational and sequential circuits in Verilog HDL*
2. *To construct user defined data types in system Verilog and create object-oriented programming environment*
3. *To demonstrate randomization and coverage concepts of system Verilog*
4. *Design and develop real-time applications using VxWorks workbench*
5. *Design and implement digital system on Zynq evaluation boards*

CYCLE - I

1. Implement a 4-bit pseudo-random Binary sequence generator using a linear feedback shift register with test bench?

2. Implement a 8-bit register with shift left and shift right modes of operation and test the logic with help of test bench?

3. Write Verilog program for cooking-gas delivery with following considerations (with signals request, wait, grant, fine)
   a) Difference between two successive deliveries should be minimum of 15 days.
   b) If user requests before 15 days, wait should be asserted
   c) If user requests when wait is asserted, fine should be asserted

4. Generate Clock signal and write Verilog code for calculating frequency of clock signal?

5. Generate clock signal and write Verilog code for skipping two clock cycles at a time and for every two clock cycles the output should be raising edge?

6. Prepare a LUT it contains the Train information such as train number, train time, number of sleeper classes and number of AC classes. Write a Verilog code when user select the Train number the output should display the train information from the prepared LUT?

7. Write SV code for
   a. Class creation
   b. Class instance and object Creation
   c. Accessing class properties and methods

d. Class Constructors

8. Write a SV code demonstrating access to static class properties and methods

9. Write a SV code for
   a. Parent class properties accessed using child class handle.
   b. Parent class method is *overridden* in the child class.

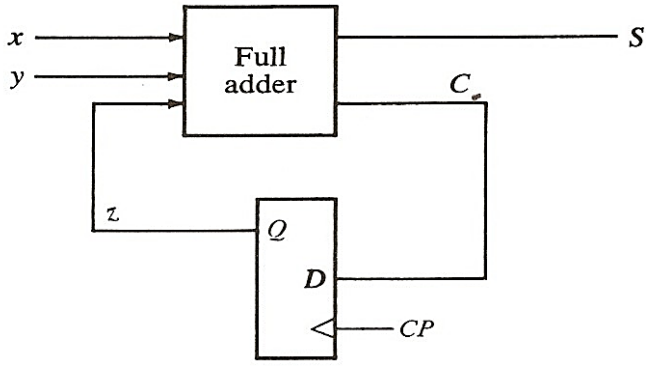
10. Write a system Verilog code to show the usage of *local* keyword and *protected* keyword within and outside a class.

11. Write a SV codes for
    a. Creating abstract classes
    b. Accessing Static class member using class resolution operator

12. Define a base class with Half Adder as a Function.
    a. Write the extended class for Full adder using the base class.
    b. Write a module defining the functionality for 4 bit Ripple carry adder.

13. Define a parent class with a 32 bit protected parameter ***tmp_addr***
    1. Write a child class containing
       i. A constructor to initialize the parameter "***tmp_addr***".
       ii. A function to increment the parameter "***tmp_addr***".
    2. Write a module showcasing the usage of protected variable "***tmp_addr***" after incrementing its address.

14. Define a base class with Full Adder as a Function.
    a. Write the extended classes for D Flipflop.
    b. Write a module defining the functionality for the following circuit.



15. Write constraint to create four random numbers **a, b, c, d**.
    i. "**a**" should be less than 5000 and greater than 100, and should not be divisible by 2
    ii. "**b**" should be less than 5,000 and should be divisible by 5
    iii. "**c**" should be in the range of 1 to 5 and include the expression [(a-b) : (a+b))]
    iv. "**d**" should be greater than all a, b and c.

16. Write a SV code for
    a. cover group

b. cover point
c. cross
d. bin

CYCLE - II

Part A: Programs Using VxWorks Workbench (Real Time Operating System)

1. Multi-Tasking
2. Round Robin Scheduling
3. Ipc Using Semaphore
4. Ipc Using Message Queues
5. Preemptive Priority Based Task Scheduling
6. Priority Inversion
7. Interrupt Service Routines

Part B: HDL Simulation & Implementation on Zynq

1. 8:1 Mux/Demux,
2. Full Adder
3. 8-bit Magnitude comparator,
4. Encoder/decoder, Priority encoder,
5. D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional),
6. 3-bit Synchronous Counters,
7. Parity generator.
8. Sequence Detector

EC 462

SEMINAR – II

Instruction: 3 periods per week *Duration of SEE: --*
CIE: 50 marks *SEE: --*
Credits: 1.5

Outcomes: At the end of this course, students will be able to**:**

1. *Develop the habit of referring the journals for literature review.*
2. *Understand the gist of the research paper.*
3. *Identify the potential for further scope.*
4. *Present the work in an efficient manner.*
5. *Write the documentation in standard format.*

Seminar topics may be chosen by the students with advice from the faculty members and the student shall read further relevant articles in the domain.

The seminar must be clearly structured and the power point presentation shall include following aspects:

1. Introduction to the field
2. Literature survey
3. Consolidation of available information
4. Summary and Conclusions
5. References

Each student is required to:

1. Deliver the seminar for a maximum duration of 30 minutes, where the presentation should be for 20 minutes in PowerPoint, followed by Question and Answers session for 10 minutes.
2. Submit the detailed report of the seminar in spiral bound in a précised format as suggested by the Department.

Guidelines for awarding marks		
S. No.	**Description**	**Max. Marks**
1	Contents and relevance	10
2	Presentation skills	10
3	Preparation of PPT slides	05
4	Questions and answers	05
5	Report in a prescribed format	20

Note:

1. The seminar presentation should be a gist of at least five research papers from **Peer-reviewed** or **UGC recognised** journals.
2. **The seminar report should be in the following order:** Background of work, literature review, techniques used, prospective deliverables, and discussion on results, conclusions, critical appraisal and reference.
3. At least two faculty members will be associated with the seminar presentation to evaluate and award marks.
4. Attendance of all the students for weekly seminar presentations is compulsory. If the student fails to secure minimum attendance as per O.U. rules, the marks awarded in the seminar presentation shall remain void.

EC 070

MINI PROJECT

Instruction: 6 periods per week *Duration of SEE: --*
CIE: 50 marks *SEE: --*
Credits: 3

Outcomes: *At the end of this course, students will be able to:*

1. *Formulate a specific problem and give solution*
2. *Develop model/models either theoretical/practical/numerical form*
3. *Solve, interpret/correlate the results and discussions*
4. *Conclude the results obtained*
5. *Write the documentation in standard format*

Guidelines:

- As part of the curriculum in the II- semester of the programme each student shall do a mini project, generally comprising about three to four weeks of prior reading, twelve weeks of active research, and finally a presentation of their work for assessment.
- Each student will be allotted to a faculty supervisor for mentoring.
- Mini projects should present students with an accessible challenge on which to demonstrate competence in research techniques, plus the opportunity to contribute something more original.
- Mini projects shall have inter-disciplinary/ industry relevance.
- The students can select a mathematical modelling based/Experimental investigations or Numerical modelling
- All the investigations should be clearly stated and documented with the reasons/explanations.
- The mini-project shall contain a clear statement of the research objectives, background of work, literature review, techniques used, prospective deliverables, and detailed discussion on results, conclusions and reference

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 50		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	20	Progress and Review
	05	Report
Departmental Committee	05	Relevance of the Topic
	05	PPT Preparation
	05	Presentation
	05	Question and Answers
	05	Report Preparation

SEMESTER - III

EC 119

ANALOG AND MIXED SIGNAL IC DESIGN
(PROGRAM SPECIFIC ELECTIVE – V)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To Design Basic Building Blocks of Opamp: Current Mirror, Single Stage Amplifiers*
- *To Design and Analyze Two-Stage Opamp and familiarize with Folded Cascade Opamps*
- *To Know Applications of Opamps and learn Data Converters and Phased Locked Loops (PLL)*

Outcomes: *At the end of this course, students will be able to:*

1. *To Develop Mathematical Modeling of Building Blocks of Opamps*
2. *To Design and Simulate Two-Stage Opamp for the Given Specifications*
3. *To Analyze the Performance of Operational Trans-Conductance Amplifier.*
4. *To Develop Switched Capacitor Circuits*
5. *To Outline the Principle of Operation of Over-Sampling Rate A/D and D/A Converters*

UNIT – I

Building Blocks of Opamp:

MOS Transistor – Nanometer Transistor and its model – body effect, Channel Length Modulation and short channel effects – velocity saturation, sub-threshold conduction, threshold voltage control, drain induced barrier lowering, gate induced drain leakage, Complete MOS Transistor Model and large and small signal models of BJTs and MOSFETs.

Current Mirrors and Single Stage Amplifiers – Simple CMOS current mirror, common source amplifier, source follower, common gate amplifier, cascade amplifiers. Source de-generated current mirrors, cascade current mirror, cascade gain stage and MOS differential pair and gain stage.

Biasing and References – Analog IC biasing, establishing constant trans-conductance and band-gap reference – Positive and negative temperature coefficient basics and circuits.

UNIT – II

*Basic Opamp and Compensation:*Basic two-stage MOS Operational amplifier, characteristic parameters, compensation, design and analysis of two-stage MOS Opamp with given specifications. Stability and frequency compensation of op-amps.

UNIT – III

Operational Trans-conductance Amplifier (OTA):

Advanced current Mirrors – Wilson current mirror, Enhanced output-impedance current mirror and gain boosting and wide swing current mirror with enhanced output impedance and bipolar current mirrors – bipolar gain stages.

Single stage Opamp – Folded-cascade Opamp, current mirror Opamp, fully differential Opamp and common mode feedback circuits.

UNIT – IV

Applications of Opamp

Comparators: Op-Amp Based Comparators, Charge Injection Errors – Latched Comparators

– CMOS and BiCMOS Comparators – Bipolar Comparators.
Switched capacitor circuits: Basic building blocks; basic operation and analysis, inverting and non-inverting integrators, signal flow diagrams, first order filter.
Sample and hold circuits - Performance requirements, MOS sample and hold basics, clock feed through problems, S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations.

UNIT – V
Mixed Signal IC Applications:
Data Converters – Review of Nyquist-Rate A/D and D/A converters, Noise Sources: Flicker, Thermal, Oversampling converters – Over sampling without noise shaping and with noise shaping, system architectures and digital decimation filters.
Phase locked loops – simple PLL, charge pump PLL and dynamics of PLL.
Practical Issues – Transistor mismatch, offset and techniques to reduce the analog non-idealities (like auto-zero, chopping, CDS etc) and Basics of Analog Layout

References:

1 Tony Chan Carusone, David Johns and Ken Martin, "*Analog Integrated Circuit Design*", 2nd edition, John Wiley & sons. 2013.
2 Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*", McGraw Hill Companies, 2013.
3 Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*", 2nd edition, Oxford University Press, 2010.

EC 118

LOW POWER VLSI DESIGN
(PROGRAM SPECIFIC ELECTIVE – V)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To study the sources of power dissipation and low power design techniques with voltage scaling and capacitance minimization approaches*
- *To study various low power arithmetic units and the design of low power multipliers*
- *To study about low power memory technologies*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand various power components*
2. *Understand and design low power memories*
3. *Understand and use mathematical models for power analysis in CMOS circuits*
4. *Design low power architectures*
5. *Realize low power low voltage adder and multipliers*

UNIT – I

*Fundamentals:*Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

*Low-Power Design Approaches***:** Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures and Circuit Level Measures.

UNIT – III

*Low-VoltageLow-Power Adders***:** Introduction, Standard Adder Cells, CMOS Adder Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles

UNIT – IV

*Low-Voltage Low-Power Multipliers:*Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier and Introduction to Wallace Tree Multiplier.

UNIT – V

*Low-Voltage Low-Power Memories***:** Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre-charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

References:

1 Sung-Mo Kang, Yusuf Leblebici, *"CMOS Digital Integrated Circuits – Analysis and Design"*, TMH, 2011.

2 Ming-BO Lin, "*Introduction to VLSI Systems: A Logic, Circuit and System Perspective",* CRC Press, 2011

3 Anantha Chandrakasan, *"Low Power CMOS Design*", IEEE Press/Wiley International, 1998

4 Kaushik Roy, Sharat C. Prasad, *"Low Power CMOS VLSI Circuit Design*", John Wiley & Sons, 2000.

5 Gary K. Yeap, "*Practical Low Power Digital VLSI Design*", Kluwer Academic Press, 2002.

EC 121

APPLICATIONS OF NANO TECHNOLOGY
(PROGRAM SPECIFIC ELECTIVE – V)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To learn the effect of nanosized materials on physical properties*
- *To learn nanotechnology concepts with rigorous scientific understanding.*
- *To learn characterizing physical properties of nano materials*
- *To learn nano material synthesis techniques*
- *To learn the applications of Nanotechnology*

Outcomes: *At the end of this course, students will be able to:*

1. *To understand the convergence of many sciences and technologies at the nanometer scale.*
2. *To serve as a standalone comprehensive introduction to applications of nanotechnology.*
3. *To explore physical characteristics of nanomaterials*
4. *To investigate newer synthesis techniques for nanomaterials*
5. *To correlate physical properties and nanosized materials*

UNIT – I

*Structure and Length Scales:*Basic properties, Examples of Crystal structures, Miller indices, Surface-to volume ratio, introduction to Length Scales, de Broglie wavelength, The Bohr radius, Excitons, Confinement regimes, Metals, The Fermi energy, Fermi velocity, and Kubo gap, The mean free path in metals, Charging energy.

UNIT – II

Types of Nanostructures and Absorption and Emission Basics: Introduction to Types of Nanostructures, Bottom-up or top-down, Exponential attenuation law, Relating ε_{molar} to σ , Estimating **α** and **σ,** using the absorption cross section, Emission processes, Einstein A and B coefficients, Relating absorption cross sections to excited-state lifetimes.

UNIT – III

A Quantum Mechanics Review: Wave functions, Observables and the correspondence principle, Eigen values and eigen functions, Wave packets, Expectation values, Dirac bra-ket notation, Operator math, The uncertainty Principle, The Schrodinger equation, The postulates of quantum mechanics, Model problems for wells, wires, and dots.

UNIT – IV

Density of States, Bands and Inter-band Transitions: Density of states for bulk materials, wells, wires and dots, Population of the conduction and valence bands , Joint density of states, The Kronig-Penney model, Metals, semiconductors, and insulators, Bulk semiconductor, Transitions in low-dimensional semiconductors.

UNIT – V

*Synthesis, Characterization and Applications***:** Molecular beam epitaxy (MBE), Colloidal growth of nanocrystals, Semiconductor nanocrystals, Sizing nanostructures, Optical characterization, Quantum dots, Metal nanostructures, Nanowires.

References:

1 Michael F. Ashby, Paulo J. Ferreira, Daniel L. Schodek, *"Nanomaterials, Nanotechnologies and Design",* Elsevier BH Publications, 2011 New Delhi.

2 Masaru Kuno, *"Introductory Nano science*", Garland Science Taylor and Francis Group, 2012, London.

3 Gabor L. Harnyak, John J. Moore, Harry F. Tibbals, Joydeep Dutta, *"Fundamentals of Nanotechnology",* CRC Press, 2008, New York

4 Ben Rogers, Sumitha Pennathur, Jesse Adams, "*Nanotechnology, Understanding Small Systems",* Second Edition CRC Press, New York, 2011.

5 K.K. Chattopadhyaya, A.N. Bannerjee, *"Introduction to Nanoscience and Nanotechnology*", PHI Learning Pvt. Ltd., New Delhi, 2012.

OE 941

BUSINESS ANALYTICS
(OPEN ELECTIVE)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *Understanding the basic concepts of business analytics and applications*
- *Study various business analytics methods including predictive, prescriptive and prescriptive analytics*
- *Prepare the students to model business data using various data mining, decision making methods*

Outcomes: *At the end of this course, students will be able to:*

1. *To understand the basic concepts of business analytics*
2. *Identify the application of business analytics and use tools to analyze business data*
3. *Become familiar with various metrics, measures used in business analytics*
4. *Illustrate various descriptive, predictive and prescriptive methods and techniques*
5. *Model the business data using various business analytical methods and techniques*

UNIT – I

*Introduction to Business Analytics :*Introduction to Business Analytics, need and science of data driven (DD) decision making, Descriptive, predictive, prescriptive analytics and techniques, Big data analytics, Web and Social media analytics, Machine Learning algorithms, framework for decision making, challenges in DD decision making and future.

UNIT – II

Descriptive Analytics: Introduction, data types and scales, types of measurement scales, population and samples, measures of central tendency, percentile, decile and quadrille, measures of variation, measures of shape-skewness, data visualization

UNIT – III

Forecasting Techniques: Introduction, time-series data and components, forecasting accuracy, moving average method, single exponential smoothing, Holt's method, Holt-Winter model, Croston's forecasting method, regression model for forecasting, Auto regression models, auto-regressive moving process, ARIMA, Theil's coefficient

UNIT – IV

Decision Trees: CHAID, Classification and Regression tree, splitting criteria, Ensemble and method and random forest. *Clustering:* Distance and similarity measures used in clustering, Clustering algorithms, K-Means and Hierarchical algorithms, *Prescriptive Analytics* - Linear Programming(LP) and LP model building,

UNIT – V

Six Sigma: Introduction, introduction, origin, 3-Sigma Vs Six-Sigma process,cost of poor quality, sigma score, industry applications, six sigma measures, DPMO, yield, sigma score, DMAIC methodology, Six Sigma toolbox

References:

1. U Dinesh Kumar, "*Data Analytics*", Wiley Publications, 1st Edition, 2017.
2. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "*Business analytics Principles, Concepts, and Applications with SAS*", Associate Publishers, 2015.
3. S. Christian Albright, Wayne L. Winston, "*Business Analytics - Data Analysis and Decision Making"*, 5th Edition, Cengage, 2015.
4. https://onlinecourses.nptel.ac.in/noc18-mg11/preview
5. https://nptel.ac.in/courses/110105089/

OE942

INDUSTRIAL SAFETY
(OPEN ELECTIVE)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Course Objectives:

- *Causes for industrial accidents and preventive steps to be taken.*
- *Fundamental concepts of Maintenance Engineering.*
- *About wear and corrosion along with preventive steps to be taken*
- *The basic concepts and importance of fault tracing.*
- *The steps involved in carrying out periodic and preventive maintenance of various equipments used in industry*

Course Outcomes:

1. *Identify the causes for industrial accidents and suggest preventive measures.*
2. *Identify the basic tools and requirements of different maintenance procedures.*
3. *Apply different techniques to reduce and prevent Wear and corrosion in Industry.*
4. *Identify different types of faults present in various equipments like machine tools, IC Engines, boilers etc.*
5. *Apply periodic and preventive maintenance techniques as required for industrial equipments like motors, pumps and air compressors and machine tools etc*

UNIT-I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes, Fire prevention and firefighting, equipment and methods.

UNIT–II

Fundamentals of Maintenance Engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT–III

Wear and Corrosion and their Prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications of Screw down grease cup, Pressure grease gun, Splash lubrication, Gravity lubrication, Wick feed lubrication, Side feed lubrication, Ring lubrication, Definition of corrosion, principle and factors affecting the corrosion, Types of corrosion, corrosion prevention methods.

UNIT–IV

Fault Tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, any one machine tool, Pump, Air compressor, Internal combustion engine, Boiler, Electrical motors, Types of faults in machine tools and their general causes.

UNIT–V

Periodic and Preventive Maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of Machine tools, Pumps, Air compressors, Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Suggested Reading:

1. H. P. Garg, "Maintenance Engineering", S. Chand and Company
2. Audels, "Pump-hydraulic Compressors", Mcgraw Hill Publication
3. Higgins & Morrow, "Maintenance Engineering Handbook", Da Information Services.
4. Winterkorn, Hans, "Foundation Engineering Handbook", Chapman & Hall London

OE 943

OPERATION RESEARCH
(OPEN ELECTIVE)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *Introduce the concepts of optimization techniques*
- *Formulation of LPP models*
- *Basic concepts of Non-linear programming, Dynamic programming, Game theory are introduced.*

Outcomes:

1. *Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.*
2. *Students should able to apply the concept of non-linear programming*
3. *Students should able to carry out sensitivity analysis*
4. *Student should able to model the real world problem and simulate it.*
5. *Student should able to apply graph theory, competitive models, and game theory simulations.*

UNIT I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT III:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT IV

Scheduling and sequencing - single server and multiple server models deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

Suggested Reading:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010.

OE 944

COST MANAGEMENT OF ENGINEERING PROJECTS
(OPEN ELECTIVE)

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- Introduce the concepts of cost management, inventory valuation , decision making
- Fundamentals of cost overruns, project execution and technical activities
- Introduce the concepts of Quantitative techniques for cost management, Linear Programming, PERT/CPM

Outcomes:

1. Understanding of strategic cost management process, control of cost and decision making based on the cost of the project.
2. Ability to appreciative detailed engineering activities of the project and execution of projects
3. Preparation of project report and network diagram
4. Able to plan Cost Behavior , Profit Planning , Enterprise Resource Planning, Total Quality Management.
5. Applications of various quantitative techniques for cost management

UNIT I

Introduction and Overview of the Strategic Cost Management Process-Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System- Inventory valuation- Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning- Project execution as conglomeration of technical and non- technical activities- Detailed Engineering activities.

UNIT III

Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT IV

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems- Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector-Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints- Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets- Performance budgets- Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V

Quantitative techniques for cost management, Linear Programming, PERT/CPM,- Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Suggested Reading :

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

OE 945

COMPOSITE MATERIALS

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To understand the fundamentals of composite materials and the role of matrix and reinforcement.*
- *To know the principles of manufacturing composite*
- *To understand the strength and failure criteria of lamina and laminate.*

Outcomes: *At the end of this course, students will be able to:*

1. *Define a composite, identify the matrix and reinforcement and highlighting the features and application of different composite materials.*
2. *Classify composites, illustrate the mechanical behaviour of composites and predict properties using micromechanics principles.*
3. *Illustrate the manufacturing of metal matrix composites and outline the properties and applications.*
4. *Illustrate the manufacturing of Polymer matrix composites and outline the properties and applications.*
5. *Apply various failure criteria to assess the strength of lamina and laminates.*

UNIT – I

Introduction: Definition- Classification and characteristics of composite materials. Advantages and applications of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, distribution, volume fraction) on overall composite performance.

UNIT – II

Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers and Boron fibers. Properties and applications of whiskers, particulate reinforcements. Mechanical Behaviour of composites: Rule of Mixtures, Inverse rule of mixtures. Isostrain and Isostress condition.

UNIT – III

***Manufacturing of Metal Matrix Composites*:** Casting-Solid State diffusion technique, Cladding-Hot Isostatic pressing, Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration-Liquid phase sintering, Manufacturing of Carbon-Carbon composites: Knitting, Braiding, Weaving, Properties and applications

UNIT – IV

***Manufacturing of Polymer Matrix Composites*:** Preparation of Moulding compounds and prepregs-hand layup method-Autoclave method-Filament winding method-Compression moulding-Reaction injection moulding, Properties and applications.

UNIT – V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hydrothermal failure. Laminate first ply failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentration.

References:

1 *Material Science and Technology*- Vol 13- Composites by R.W. Cahn-VCH, West Germany.
2 *Materials Science and Engineering, An Introduction*. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley &Sons, NY, Indian edition, 2007.
3 *Composite Materials*- K. K. Chwala.
4 *Composite Materials Science and Applications*-Deborah D.L. Chung.
5 *Composite Materials Design and Applications*-Danial Gay, Suong V. Hoa and Stwphen W. Tsai.

OE 946

WASTE TO ENERGY

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*
Credits: 3

Objectives:

- *To know the various forms of waste*
- *To understand the processes of Biomass Pyrolysis.*
- *To learn the technique of Biomass Combustion.*

Outcomes: *At the end of this course, students will be able to:*

1. *Understand the concept of conservation of waste*
2. *Identify the different forms of wastage*
3. *Choose the best way for conservation to produce energy from waste*
4. *Explore the ways and means of combustion of biomass*
5. *Develop a healthy environment for the mankind*

UNIT – I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based,Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

UNIT – II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal –Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT – III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraftgasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT – IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT – V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

References:

1 *Non Conventional Energy*, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2 *Biogas Technology - A Practical Hand Book* - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3 *Food, Feed and Fuel from Biomass,* Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4 *Biomass Conversion and Technology*, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

OE947

INTERNET OF THINGS
(Open Elective)

Instruction: 3periods per week | Duration of SEE: 3 hours
CIE: 30 marks | SEE: 70 marks
Credits: 3

Course Objectives:

- To understand the concepts of Internet of Things and able to build IoT applications
- To learn the programming and use of Arduino and Raspberry Pi boards.
- To know about data handling and analytics in SDN.

Course Outcomes:

After Completion of the course Student will be able to:

1. Known basic protocols in sensor networks.
2. Program and configure Arduino boards for various designs.
3. Python programming and interfacing for Raspberry Pi.
4. Design IoT applications in different domains.

UNIT – I

Introduction to Internet of Things, Characteristics of IoT, Physical design of IoT, Functional blocks of IoT, Sensing, Actuation, Basics of Networking, Communication Protocols, Sensor Networks.

UNIT – II

Machine-to-Machine Communications, Difference between IoT and M2M, Interoperability in IoT, Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino,

UNIT – III

Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi

UNIT - IV

Implementation of IoT with Raspberry Pi, Introduction to Software defined Network (SDN), SDN for IoT, Data Handling and Analytics,

UNIT - V

Cloud Computing, Sensor-Cloud, Smart Cities and Smart Homes, Connected Vehicles, Smart Grid, Industrial IoT, Case Study: Agriculture, Healthcare, Activity Monitoring

Suggested Readings:

1. "The Internet 'of Things: Enabling Technologies, Platforms, and Use Cases", by PethuruRaj and Anupama C. Raman (CRC Press).
2. “Make sensors”: Terokarvinen, kemo, karvinen and villeyvaltokari, 1st edition, maker media, 2014.
3. "Internet of Things: A Hands-on Approach", by ArshdeepBahga and Vijay Madisetti Vijay Madisetti,
4. ArshdeepBahga, “Internet of Things: A Hands-On Approach”
5. WaltenegusDargie,ChristianPoellabauer, "Fundamentals of Wireless Sensor Networks: Theory and Practice"
6. Beginning Sensor networks with Arduino and Raspberry Pi – Charles Bell, Apress, 2013

OE948

CYBER SECURITY

(Open Elective)

Instruction: 3periods per week | Duration of SEE: 3 hours
CIE: 30 marks | SEE: 70 marks
Credits: 3

Course Objectives

- Learn the various threats in networks and security concepts.
- Apply authentication applications in different networks.
- Understand security services for email.
- Awareness of firewall and IT laws and policies

Course Outcomes:

After completion of this course, the students shall be able to:

1. Understand the various network threats.
2. Analyze the forensic tools for evidence collection.
3. Apply the firewalls for threat analysis.

UNIT-I

Ethical hacking, Attack Vectors, Cyberspace and Criminal Behaviour, Clarification of Terms, Traditional Problems associated with Computer Crimes, Realms of Cyber world, brief history of the internet, contaminants and destruction of data, unauthorized access, computer intrusions, white-collar crimes, viruses and malicious code, virus attacks, pornography, software piracy, mail bombs, exploitation, stalking and obscenity in internet, Cyber psychology, Social Engineering.

UNIT-II

Introduction to Digital forensics, Forensic software and handling, forensic hardware and handling, analysis and advanced tools, forensic technology and practices, Biometrics: face, iris and fingerprint recognition, Audio-video evidence collection, Preservation and Forensic Analysis.

UNIT-III

Investigation Tools, e-discovery, EDRM Models, digital evidence collection and preservation, email investigation, email tracking, IP tracking, email recovery, searc and seizure of computer systems, password cracking.

UNIT-IV

Forensic Analysis of OS artifact, Internet Artifacts, File System Artifacts, Registry Artifacts, Application Artifacts, Report Writing, Mobile Forensic- identification, collection and preservation of mobile evidences, social media analysis, data retrival, Email analysis from mobile phones.

UNIT-V

Ethics, Policies and IT Act Basics of Law and Technology, Introduction to Indian Laws, Scope and Jurisprudence, Digital Signatures, E Commerce-an Introduction, possible crime scenarios, law coverage, data interchange, mobile communication development, smart card and expert systems Indian Laws, Information Technology Act 2000, Indian Evidence Act, India Technology Amendment Act 2008, Indian Penal Code , Computer Security Act 1987, National Information Infrastructure Protection Act 1996, Fraud Act 1997, Children Online Protection Act 1998, Computer Fraud and Abuse Act 2001, Intellectual Property, IP Theft, Copyright, Trademark, Privacy and Censorship, Introduction to Cyber Ethics, rights over intellectual property, Corporate IT Policy Formulations, Compliance Auditing.

Suggested Readings

1. Charles P. Fleeger, "*Security in Computing*", Prentice Hall, New Delhi, 2009.
2. BehrouzA.Forouzan, "*Cryptography & Network Security*", Tata McGraw Hill, India, New Delhi, 2009.
3. William Stallings, "*Cryptography and Network Security*", Prentice Hall, New Delhi, 2006.
4. Chalie Kaufman, Radia Perlman, Mike Speciner, "*Network Security: Private Communication in a Public Network*", Pearson Education, New Delhi, 2004.
5. Neal Krawetz, "*Introduction to Network Security*", Thomson Learning, Boston, 2007.
6. Bruce Schneier, "*Applied Cryptography*", John Wiley & Sons, New York, 2004.

EC 481

MAJOR PROJECT PHASE - I

Instruction: 20 periods per week *Duration of SEE: --*
CIE: 100 marks *SEE: --*
Credits: 10

Outcomes: *At the end of this course, students will be able to:*

1. *Exposed to self-learning various topics.*
2. *Learn to survey the literature such as books, journals and contact resource persons for the selected topic of research.*
3. *Learn to write technical reports.*
4. *Develop oral and written communication skills to present.*
5. *Defend their work in front of technically qualified audience*

Guidelines:

- The Project work will preferably be a problem with research potential and should involve scientific research, design, generation/collection and analysis of data, determining solution and must preferably bring out the individual contribution.
- Seminar should be based on the area in which the candidate has undertaken the dissertation work.
- The CIE shall include reviews and the preparation of report consisting of a detailed problem statement and a literature review.
- The preliminary results (if available) of the problem may also be discussed in the report.
- The work has to be presented in front of the committee consists of Chairperson-BoS, Osmania University and Head, Supervisor & Project coordinator from the respective Department of the Institute.
- The candidate has to be in regular contact with his supervisor and the topic of dissertation must be mutually decided by the guide and student.

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	30	Project Status / Review(s)
	20	Report
Departmental Committee (Chairperson BoS, Osmania University and Head, Supervisor & Project coordinator from the respective department of the institution)	10	Relevance of the Topic
	10	PPT Preparation
	10	Presentation
	10	Question and Answers
	10	Report Preparation

Note: The Supervisor has to assess the progress of the student regularly.

SEMESTER - IV

EC 482

MAJOR PROJECT PHASE - II

Instruction: 32 periods per week *Duration of SEE: --*
CIE: -- *SEE: 200 marks*
Credits: 16

Outcomes: *At the end of this course, students will be able to:*

1. *Use different experimental techniques and will be able to use different software/ computational /analytical tools.*
2. *Design and develop an experimental set up/ equipment/test rig.*
3. *Conduct tests on existing set ups/equipment and draw logical conclusions from the results after analysing them.*
4. *Either work in a research environment or in an industrial environment.*
5. *Conversant with technical report writing and will be able to present and convince their topic of study to the engineering community.*

Guidelines:

- It is a continuation of Major Project Phase – I started in semester - III.
- The student has to submit the report in prescribed format and also present a seminar.
- The dissertation should be presented in standard format as provided by the department.
- The candidate has to prepare a detailed project report consisting of introduction of the problem, problem statement, literature review, objectives of the work, methodology (experimental set up or numerical details as the case may be) of solution and results and discussion.
- The report must bring out the conclusions of the work and future scope for the study. The work has to be presented in front of the examiners panel consisting of an approved external examiner and Chairperson BoS, & Head, Osmania University and Supervisor from the Institute.
- The candidate has to be in regular contact with his/her Supervisor / Co- Supervisor

Guidelines for awarding marks in SEE (Semester End Examination): Max. Marks: 200		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	30	Quality of the work which may lead to publications
	10	Analytical / Programming / Experimental Skills Preparation
	10	Report preparation in a standard format
External Examiner and Chairperson, BoS & Head, Osmania University (All together	20	Power Point Presentation
	60	Quality of thesis and evaluation
	30	Innovations, application to society and Scope for future study
	20	Viva-Voce