PRESS RELEASE

Osmania University set a record by developing Indigenous semiconductor Chip for the first time in the history of state level universities in India. Prof. Kumar Molugaram, Hon'ble Vice Chancellor of Osmania University launched the fabricated Semiconductor chip

Hyderabad, July 25, 2025:

In a major stride toward self-reliant semiconductor innovation, Osmania University, in collaboration with Chaitanya Bharathi Institute of Technology (CBIT), has **successfully developed and fabricated a prototype** of All-Digital Phase-Locked Loop (ADPLL) ASIC chip under the Chips to Startup (C2S) programme, supported by the Ministry of Electronics and Information Technology (MeitY) and the Centre for Development of Advanced Computing (CDAC), Govt. of India. As part of this initiative, the team successfully fabricated the ADPLL chip using 180 nm CMOS technology at Semiconductor Laboratory (SCL), Mohali. This marks a significant milestone in leveraging domestic semiconductor infrastructure for advanced ASIC design and fabrication. This accomplishment reflects the spirit of *Aatmanirbhar Bharat* and showcases the capacity of Indian academia to deliver high-resolution, silicon-proven IP cores for next-generation electronic systems.

Prof. Kumar Molugaram, Hon'ble Vice Chancellor of Osmania University **formally unveiled the fabricated ADPLL chip on July 25, 2025** in the presence of Academic Council members, university officials, Prof. P. Chandra Sekhar, Principal, UCEOU, Prof. A. Krishnaiah, Dean, Faculty of Engineering, Prof. B. Mangu, Vice-Principal, UCEOU, Prof. B. Rajendra Naik, Dean, Student affairs, OU, Prof. P. Naveen Kumar, Head, Department of ECE, Heads and BoS chairpersons of various Departments, and the project team.

On this occasion, the Vice Chancellor appreciated the efforts of the team led by Prof. P. Chandra Sekhar, Principal Investigator, and commended the Professor for his leadership and for successfully securing this **prestigious project of Rs. 5 Crores under the C2S programme** and creating a Centre of Excellence in Artificial Intelligence and Integrated circuits (CIIC). Prof. Kumar assured to extend the support for the facilities and industrial collaborations. He directed all the faculty members to achieve such prestigious projects in the same lines.

Prof. P. Chandrasekhar expressed his sincere gratitude to MeitY and CDAC for their continued support in providing full-fledged EDA tools Cadence, Synopsys and for IC fabrication. He thanked Hon'ble Vice Chancellor for his support and congratulated his team members Dr. Jahangeer, Assistant Professor, CBIT and Mr. Misbahuddin, Assistant Professor, Osmania University. He thanked the BE ECE 1983 batch for providing the servers worth Rs. 50 lakhs and CHAVASK for providing GPGPU servers worth Rs. 50 lakhs. He briefed the roadmap for the development of a complete ADPLL System-on-Chip (SoC), Agriculture and Healthcare sensors with the support of CHAVASK and BITSILICA, marking a step forward in commercializing indigenous semiconductor IP course.

Principal