Day 1 (Friday, August 31)

20:00-3:15 Overview of Open Computing Language (OpenCL)
Dr P Chandrasekhar &
Prof S Ramachandram, UCE

OpenCL is a framework for writing programs that execute across heterogeneous platforms consisting of central processing unit (CPU), graphics processing unit (GPU), and other processors. OpenCL includes a language for writing kernels (functions that execute on OpenCL devices), plus application programming interfaces (APIs) that are used to define and then control the platforms. OpenCL provides parallel computing using task-based and data-based parallelism. The lecture will be followed by demonstration of example applications.

3:15-3:35 Tea Break

3:35-5:15 Parallel Programming w/ OpenCL
AND AMD APP SDK TOOLS
Mr Sushant Kumar &
Mr Srinivasa Charupalli, AMD

This talk is on AMD APP Software Development Kit (SDK). AMD APP SDK is a complete development platform created by AMD to allow you to quickly and easily develop applications accelerated by AMD APP technology. The SDK allows you to develop your applications in a high-level language, OpenCL™ (Open Computing Language)

Day 2 (Saturday, September 1)

9:00-10:00 Heterogeneous Computing Platforms Used in Satellite Data Processing to Achieve High Performance
Dr K Pramod Kumar, Scientist & Division Head HPC, Dept. of Space, ADRIN, India

This talk briefly describes issues and complexities involved in Satellite data processing and use of heterogeneous platforms- FPGAs, CPUs and multicore CPUs for overcoming the data exodus and also achieving high performance. Use of Open Standards minimize many of the issues such as hardware-software integration, programming complexity, debugging and maintenance but also pose some other challenges.

10:00-10:55 Reconfigurable Computing Platform for Embedded Systems
Mr K Arunababu, Scientist E, ANURAG,
DRDO, India

This talk describes FPGA based reconfigurable systems that can be used for Embedded Processing in High-end applications like Multi-mode Multi-Service Radio, Stereoscopic Visualization and Pattern Recognition. These applications demand more computational power, higher logic functionality, and stringent timing behavior. Benefits of run-time re-configurability for performance are discussed.

10:55-11:15 Tea Break

11:15-12:15 Efficient Hardware Software Partitioning using ADI DSP
Mr Rajesh Mahapatra, Senior Engineering Manager, Analog Devices

The complexity that a Digital Signal Processor handles today is huge. Increasing core complexity or speed is not the only solution. Efficient partitioning of work load between hardware and software is one elegant way of solving this problem. ADI’s latest Blackfin DSP solves some of the MIPS hungry algorithms that is typical in imaging and video processing in a very elegant manner. These approaches are discussed in addition to a brief introduction of the architecture of the new Blackfin DSPs from Analog Devices.

12:15-1:15 Open Source Solutions for the Zynq - All Programmable SOC
Prasobh Mohananalichamy, Senior Product Marketing Engineer, Xilinx

The Zynq-7000 family combines an ARM® dual-core Cortex™-A9 MPCore™ processing system with programmable logic on a single chip. This architecture allows the device to boot like a processor and load custom hardware or accelerators when the CPU is running. This class of All Programmable device gives designers increased flexibility, performance and BOM cost reduction. But there are challenges in programming these new class of Heterogeneous Systems. This session focuses on listing the various challenges from Hardware-Software partitioning to addressing these challenges to design an optimized system by leveraging open source or industry standard tools and frameworks.

1:15-2:00 Lunch (Served)