**SCHEME OF INSTRUCTION**
M.TECH (EMBEDDED SYSTEMS AND COMPUTING)
Proposed from the Academic year 2016-17

**SEMESTER - I**

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course Code</th>
<th>Course Title</th>
<th>Scheme of Instruction</th>
<th>Contact Hrs/Wk</th>
<th>Scheme of Examination</th>
<th>Credits</th>
</tr>
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<tbody>
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**Departmental Requirements**

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**Total**

| 18 | 6 | 24 | 280 | 420 | 22 |

**SEMESTER - II**

<table>
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<tr>
<th>S.No</th>
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**Departmental Requirements**

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</table>

**Total**

| 18 | 6 | 24 | 280 | 420 | 22 |
**SCHEME OF INSTRUCTION**
M.TECH (EMBEDDED SYSTEMS AND COMPUTING)
Proposed from the Academic year 2016-17

**SEMESTER III**

<table>
<thead>
<tr>
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<th>Contact Hrs/Wk</th>
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**Project Seminar Evaluation:** 50 marks to be awarded by Supervisor and 50 marks to be awarded by Viva-Voce committee comprising Head, Supervisor and an Examiner.

**SEMESTER – IV**

<table>
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<tr>
<th>S. No</th>
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**Note:** Six Core subjects, Six Elective subjects, Two Laboratory Courses and Two Seminars must be offered in Semester I and II.
With effect from the Academic Year 2016 – 2017

# List of Core Subjects:

<table>
<thead>
<tr>
<th>S.No</th>
<th>Course Code</th>
<th>Course Title</th>
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<tr>
<td>1</td>
<td>CS 5301</td>
<td>Embedded System Design</td>
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<tr>
<td>2</td>
<td>CS 5302</td>
<td>Digital System Design</td>
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<tr>
<td>3</td>
<td>CS 5303</td>
<td>Microcontrollers for Embedded Systems</td>
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<tr>
<td>4</td>
<td>CS 5304</td>
<td>Real Time Operating Systems</td>
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<tr>
<td>5</td>
<td>CS 5305</td>
<td>Simulation and Modeling</td>
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<tr>
<td>6</td>
<td>CS 5306</td>
<td>Hardware and Software Co-design</td>
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*List of Elective Subjects:

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<tr>
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<td>Multimedia Technologies</td>
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<tr>
<td>2</td>
<td>CS5101</td>
<td>Advanced Algorithms</td>
</tr>
<tr>
<td>3</td>
<td>CS5351</td>
<td>Advanced Computer Architecture</td>
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<tr>
<td>4</td>
<td>CS5352</td>
<td>Scripting Languages for Design Automation</td>
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<td>5</td>
<td>CS5353</td>
<td>Software Engineering for Real Time Systems</td>
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<tr>
<td>6</td>
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<td>Embedded Programming</td>
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<tr>
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<td>CS5363</td>
<td>Reliability and Fault Tolerance</td>
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<td>16</td>
<td>CS5364</td>
<td>Performance Evaluation of Computer Systems</td>
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</table>
CS 5301  EMBEDDED SYSTEM DESIGN

Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT-I


UNIT-II

Embedded Hardware Design and Development: VLSI and Integrated Circuit Design, EDA tools, usage of EDA tools and PCB layout.

Embedded Firmware Design and Development: Embedded firmware Design approaches and Development languages. Examples of Embedded Systems, Design Metrics in Embedded System

UNIT-III


UNIT-IV

Introduction to Real Time Operating Systems: Tasks and Task States, Tasks and Data, Semaphores, and Shared Data; Message Queues, Mailboxes and Pipes, Timer Functions, Events, Memory Management, Interrupt Routines in an RTOS Environment. OS security issues and Mobile OS.

UNIT-V


Suggested Reading:
UNIT-I

Analysis & Design of Combinational Logic: Introduction to combinational circuits, code conversions, decoder, encoder, priority encoder, multiplexers as function generators, binary adder, subtractor, BCD adder, Binary comparator, arithmetic logic units.

UNIT-II

Design of Sequential Circuits- Derivation of State diagrams and tables, transition table, excitation table and equations. Analysis of simple synchronous sequential circuits, construction of state diagram, counter design with state equations, Registers, serial in serial out shift registers, tristate register, timing considerations.

UNIT-III


UNIT-IV

Design options of Digital Systems: Programmable logic devices, programmable read only memory, programmable logic arrays and programmable array logic, Design using PLA, PAL, and Field Programmable Gate Arrays. Synthesis: Design flow of ASICs and FPGA based system.

UNIT-V


Suggested Reading:

CS5303 MICROCONTROLLERS FOR EMBEDDED SYSTEMS

Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT–I


UNIT – II

Comparison of various families of 8-bit microcontrollers, Interfacing of LCD, ADC, DAC, Sensors and Keyboard using Microcontrollers, USB and RS232.

UNIT – III

Introduction: RISC/ARM Design Philosophy and Functional Block Diagram. Programmers Model: Data Types, Processor modes, Registers, General Purpose Registers, Program Status Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table, and ARM Processor Families.

UNIT – IV

ARM9 Microcontroller Architecture: Block Diagram, Features, Memory Mapping, Memory Controller (MC), External Bus Interface (EBI), Connections to Memory Devices System Timer (ST): Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT), Real Time Clock (RTC), and Parallel Input/Output Controller (PIO).

UNIT- V


Suggested Reading:
CS5304 REAL TIME OPERATING SYSTEMS
Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT I


Portable Operating System Interface (POSIX) – IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability.

UNIT II


UNIT III


UNIT IV

VxWorks – POSIX Real Time Extensions, timeout features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues, Memory Management – Virtual to Physical Address Mapping.

UNIT V

Debugging Tools and Cross Development Environment – Software Logic Analyzers, ICES.

Comparison of RTOS – VxWorks, μC/OS-II and RT Linux for Embedded Applications.

Suggested Reading:

With effect from the Academic Year 2016 – 2017

CS5305  SIMULATION AND MODELING
Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT-I


UNIT-II

Overview of Statistical Models and Queuing Systems
Programming languages for Simulation: Continuous and discrete Simulation Languages – FORTRAN, GPSS, SIMAN, SIMSCRIPT, SLAM and MODSIM.

UNIT-III


UNIT-IV

Input Data Analysis: Data Collection: Identify the distribution, Parameter & Estimation. Goodness of fit tests: Chi Square Test – KS test; Multivariate and time series input models, Verification and Validations of simulation models, Model building, Verification and Validation: Verification of Simulation Models: Calibration and Validation of Models Face Validity, Validation of Model Assumptions, Validation Input/Output Transformations, Input/Output Validation using Historical input data, Input/Output validation sing Turning Test.

UNIT-V

Suggested Reading:

CS5306 HARDWARE AND SOFTWARE CO-DESIGN
Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I

Introduction: Issues in co-designs, models, architectures, languages and generic co-design methodology.

UNIT-II

Hardware / Software co-synthesis Algorithms: Introduction, architecture models, hardware/software partitioning, distributed system co-synthesis.

UNIT-III

Prototyping and Emulation: Introduction, prototyping and emulation techniques, prototyping and emulation environments and future developments in emulation and prototyping.

UNIT-IV

Compilation Techniques and Tools for Embedded processor architectures: Introduction, Modern embedded architectures, embedded software development needs, compilation techniques, practical considerations in a compiler development environment.

UNIT-V


Suggested Reading:

With effect from the Academic Year 2016 – 2017

CS 5321 SOFTWARE LAB-I
Credits: 2

Instruction: (3L) hrs per week
CIE: 50 marks


I. Implement the following using 8051, ARM7/ARM9 and Embedded C:
   1) Experiments based on I/O Port, Timer, Serial & Interrupt Program using Keil (or equivalent) IDE.
   2) Experiments on:
      i. Digital Interfaces  
      ii. LCD Display interfaces  
      iii. Analog Interfaces  
      iv. Keyboard Interfaces  
      v. PC –Interface with RS232, Ethernet etc.,  
      vi. Stepper motor, traffic light controller, sensor devices etc.,

   i. Combinational Circuits  
   ii. Sequential Circuits and FSMs  
   iii. Case study (Complete FPGA design flow including on-chip debugging)

Suggested Tools: Xilinx ISE/Altera Quartus, Modelsim/Active HDL and Target boards.

Note: The students have to submit a report using LateX at the end of the semester.

Suggested Reading:

Note: The students have to submit a report at the end of the semester.
CS 5322

SEMINAR - I

Credits: 2

Instruction: (3L) hrs per week
CIE: 50 marks

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for systematic independent study of state of the art topics in broad area of his/her specialization.

Seminar topics can be chosen by the students with the advice from the faculty members. Students are to be exposed to following aspects of seminar presentations.

- Literature survey
- Organization of material
- Preparation of Power point Presentation slides
- Technical writing

Each student is required to

1. Submit one page of synopsis of the seminar talk two days before for display on notice board.
2. Give 20 minutes presentation through MS-PowerPoint Presentation Slides followed by 10 minutes discussion.
3. Submit a report on the seminar topic with a list of references and slides used within a week.

Seminars are to be scheduled from the 3rd week of the last week of the semester and any change in schedule should be discouraged.

The CIE marks will be awarded to the students by atleast 2 faculty members on the basis of oral presentation and report as well as their involvement in the discussion.
CS 5323 SOFTWARE LAB – II

Credits: 2

Instruction: (3L) hrs per week
CIE: 50 marks

Programs based on usage of UNIX commands, System Calls, Shell programming.

1. Program that makes a copy of a file using standard I/O and system calls (using command line arguments)
2. Program to implement ‘cat’ command using system calls
3. Program to implement ‘ls’ command using system calls
4. Program that takes one or more file/directory names as command line input and reports the following information on the file.
   A. File type.
   B. Number of links.
   C. Time of last access.
   D. Read, Write and Execute permissions.
5. Program to create a child process and allow the parent to display “parent” and the child to display child” on the screen.
6. Write a program to create a Zombie process.
7. Write a program that illustrates how an orphan is created.
8. Write a program that illustrates how to execute two commands concurrently with a command pipe.
9. Write a program that illustrates suspending and resuming processes using signals.
10. Write a program to implement IPC using unnamed pipes (anonymous pipe)
11. Write a program to implement half duplex communication between two unrelated processes using named pipe (FIFO)
12. Write programs to demonstrate message queue IPC
13. Write a program that illustrates two processes communicating using shared memory.
14. Write a Program that demonstrate semaphores
15. Write a C program to demonstrate multi threading

Note: The students have to submit a report at the end of the semester.
CS 5324 SEMINAR –II

Credits: 2

Instruction: (3L) hrs per week
CIE: 50 marks

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the student for systematic independent study of state of the art topics in broad areas of his/her specialization.

Seminar topics can be chosen by the students with the advice from the faculty members.

Students are to be exposed to following aspects of seminar presentation.

Literature Survey

Organization of material

Preparation of Power point Presentation slides and Technical Writing.

Each Student is required to:

1. Submit one page of synopsis of the seminar talk two days before for display on notice board.
2. Give 20 minutes presentation through MS-Power Point presentation slides followed by 10 minutes discussion.
3. Submit a report on the seminar topic with a list of references and slides used within a week.

Seminar are to be scheduled from the 3rd week to the last week of the semester and any change in schedule should be discouraged.

The CIE marks will be awarded to the students by atleast 2 faculty members on the basis of oral and a written presentation as well as their involvement in the discussion.
With effect from the Academic Year 2016 – 2017

CS5054 MULTIMEDIA TECHNOLOGIES
Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks

Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I

Media and Data Streams: Properties of multimedia systems, Data streams characteristics: Digital representation of audio, numeric instruments digital interface Bark concepts, Devices, Messages, Timing Standards Speech generation, analysis and transmission.

UNIT-II

Digital Image: Analysis, recognition, transmission, Video: Representation, Digitalization transmission Animations: Basic concepts, animation languages, animations control transmission

UNIT-III

Data Compression Standards: JPEG, H-261, MPEG DVI

Optical storage devices and Standards: WORHS, CDDA, CDROM, CDWO, CDMO.

Real Time Multimedia, Multimedia file System.

UNIT-IV

Multimedia Communication System: Collaborative computing session management, transport subsystem, QOS, resource management.

Multimedia Databases: Characteristics, data structures, operation, integration in a database model. A Synchronization: Issues, presentation requirements, reference to multimedia synchronization, MHEG

UNIT-V

Multimedia Application: Media preparation, Composition, integration communication, consumption, entertainment.

Suggested Reading:

CS 5101  ADVANCED ALGORITHMS

Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I

Algorithm Analysis: Asymptotic Notation, Amortization.

Basic Data Structures: Stacks and Queues, Vectors, Lists and Sequences, Trees, Priority Queues, Heaps, Dictionaries and Hash Tables.


UNIT-II


Graphs: The Graph Abstract Data Type, Data Structures for Graphs, Graph Traversal, Directed Graphs.

UNIT-III


UNIT-IV


UNIT-V

Suggested Reading:

CS5351 ADVANCED COMPUTER ARCHITECTURE
Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I
Measuring Performance and cost: Performance measurement, Enhancements to Uni processor models, Benchmarks, Basic model of advanced computer architectures.

UNIT-II
Pipelining and superscalar techniques: Basic pipelining, data and control hazards, Dynamic instruction scheduling, Branch prediction techniques, Performance evaluation, case study- Sun Microsystems -Microprocessor.

UNIT-III

UNIT-IV

UNIT-V
Multiprocessors and Multi computers: Multiprocessor models, Shared-memory and distributed memory architectures, memory organization, Cache Coherence and Synchronization Mechanisms, parallel computer, performance models.

Suggested Reading:
CS5352  SCRIPTING LANGUAGES FOR DESIGN AUTOMATION

Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT I
Overview of scripting languages- PERL, file handles, operators, control structures, regular expressions, built in data types, operators, statements and declarations- simple, compound, loop statements, global and scoped declarations.

UNIT II
Pattern matching - regular expression, pattern matching operators, character classes, positions, capturing and clustering.

UNIT III
Subroutines- syntax, semantics, proto types, format variables, references, data structures- arrays of arrays, hashes of arrays, hashes of functions.
Inter process communication- signals, files, pipes, sockets.

UNIT IV
Threads- process model, thread model, perl debugger- using debugger commands, customization, internals and externals, internal data types, extending perl, embedding perl, exercises for programming using perl.

UNIT V
Java Script: Introduction to Java Script, Data types, Arithmetic’s Equality relational, assignment increment, decrement operators, Java Script Control Structures – if, if-else, while.

Java Script Control Structures: For, Switch, Do/While, break. Programming modules, recursion, recursion vs iteration global functions arrays, using arrays, Reference and reference parameters, passing arrays to functions, multiplesubscripted arrays, objects-math, string, Boolean and number.

Suggested Reading:

CS5353 SOFTWARE ENGINEERING FOR REAL TIME SYSTEMS  
Credits: 3

Instruction: (3L) hrs per week  
CIE: 30 marks  
Duration of SEE: 3 hours  
SEE: 70 marks

UNIT-I


UNIT-II


UNIT-III


UNIT-IV


UNIT-V


Suggested Reading:

CS5354          EMBEDDED PROGRAMMING

Credits: 3

Instruction: (3L) hrs per week          Duration of SEE: 3 hours
CIE: 30 marks                             SEE: 70 marks

UNIT-I
Booting Process in Linux GNU Tools: gcc, Conditional Compilation, Preprocessor directives, Command line arguments, Make files

UNIT-II
Embedded C Programming, Review of data types - Scalar types-Primitive types-Enumerated types- Subranges, Structure types-character strings -arrays- Functions
Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly. Embedded programming issues - Reentrancy, Portability, Optimizing, and testing embedded C programs.

UNIT-III
Embedded Applications using Data structures , Linear data structures- Stacks and Queues Implementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, and non-linear structures.

UNIT-IV
Introduction to Object Oriented Concepts, Core Java/Java, Core- Java buzzwords, Overview of Java programming, Data types, variables and arrays, Operators, and Control statements.

UNIT-V
Embedded Java - Understanding J2ME,Connected Device configuration, Connected Limited device configuration, Profiles, Anatomy of MIDP applications, and Advantages of MIDP.

Suggested Reading:
CS 5355  FIELD PROGRAMMABLE GATE ARRAYS

Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT-I

Introduction to ASIC: Types of ASIC’s, ASIC design flow, Economics of ASIC’s, Programmable ASIC’s: CPLD and FPGA. Commercially available CPLD’s and FPGA’s: XILINX, ALTERA, ACTEL. FPGA Design cycle, Implementation tools: Simulation and synthesis, and Programming technologies.

UNIT-II

FPGA logic cell for XILINX, ALTERA and ACTEL ACT, Technology trends, AC/DC IO Cells, clock and power inputs, FPGA interconnect: Routing resources, Elmore’s constant, RC delay and parasitic capacitance FPGA design flow, and Low-level design entry.

UNIT-III

FPGA physical design, CAD tools, Power dissipation, FPGA Partitioning, Partitioning methods, Floor planning: Goals and objectives, I/O, Power and clock planning, and Floor Planning tools.

UNIT-IV

Placement: Goals and objectives, Placement algorithms: Min-cut based placement, Iterative Improvement, and simulated annealing.

Routing: Goals and objectives, Global routing methods, Back-annotation. Detailed Routing: Goals and objectives, Channel density, Segmented channel routing, Maze routing, Clock and power routing, Circuit extraction, and DRC.

UNIT-V


Suggested Reading:

CS5356 SYSTEM-ON CHIP ARCHITECTURE
Credits: 3

Instruction: (3L) hrs per week Duration of SEE: 3 hours
CIE: 30 marks SEE: 70 marks

UNIT-I


UNIT-II


UNIT-III

Memory Hierarchy: Memory size and speed – On-chip memory Caches –Cache design- an example- memory management.

UNIT-IV


UNIT-V


Suggested Reading:

CS 5357  
**OPTIMIZATION TECHNIQUES**

*Credits: 3*

*Instruction: (3L) hrs per week*  
*CIE: 30 marks*  
*Duration of SEE: 3 hours*  
*SEE: 70 marks*

**UNIT-I**

Use of optimization methods. Introduction to classical optimization techniques, motivation to the simplex method, simplex algorithm, sensitivity analysis.

**UNIT-II**


**UNIT-III**

Descent methods, Gradient of function, steepest decent method, conjugate gradient method.


**UNIT-IV**

Review of a global optimization techniques such as Monte Carlo method, Simulated annealing and Tunneling algorithm.

**UNIT V**

Generic algorithm - Selection process, Crossover, Mutation, Schema theorem, comparison between binary and floating point implementation.

**Suggested Reading:**

CS5358 PRODUCT DESIGN AND QUALITY MANAGEMENT

Credits: 3

Instruction: (3L) hrs per week  
Duration of SEE: 3 hours
CIE: 30 marks  
SEE: 70 marks

UNIT-I

UNIT-II

UNIT-III

UNIT-IV

UNIT-V
Total Quality Management, Quality Function Deployment, Product Liability, Failure Mode and Effect Analysis, Management Tools.

Suggested Reading:
CS5359  
DESIGN FOR TESTABILITY  
Credits: 3

Instruction: (3L) hrs per week  
Duration of SEE: 3 hours  
CIE: 30 marks  
SEE: 70 marks

UNIT -I


UNIT –II


UNIT –III


UNIT –IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT –V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Suggested Reading:
CS5360 DSP - ARCHITECTURE

Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks    SEE: 70 marks

UNIT I
Introduction to DSP Processors: Differences between DSP and other µp architectures, their comparison and need for special ASPs, RISC & CISC CPUs.

UNIT II
Overview of DSP processor design: fixed point DSPs – Architecture of TMS 320C 5X, C54X Processors, addressing modes, Assembly instructions, Pipelining and on-chip peripherals.

UNIT III
Floating point DSPs: Architecture of TMS 320 – IX- Data formats, Floating Point operations, addressing modes, instructions, pipelining and peripherals.

UNIT IV
DSP interfacing & software development tools: I/O interfacing with A/D converters, PCs, Dual port RAMs, EPGAs, DSP tools – Assembler, debugger, c-compiler, linker, editor, code composer studio.

UNIT V
Applications using DSP adaptive filtering, spectrum analysis, Echo cancellation modems, voice synthesis and recognition. Brief ideas of AD, Motorola DSP CPUs and their comparison with TI CPUs.

Suggested Reading:

CS5361 GRAPH THEORY AND ITS APPLICATIONS

Credits: 3

UNIT I

Introduction: Graphs and Simple graphs, Graph isomorphism, Representation of Graphs, Sub graphs, Degree sequences, Basic properties of graphs, Graph traversals-DFS, BFS algorithms.

UNIT II

Trees and Connectivity: Trees, Cut Edges and Bonds, Cut Vertices, Gayley’s Formula, Bridges and blocks, Euler Tours, Hamilton Cycles. Minimum spanning tree and maximum spanning tree algorithms.

UNIT III

Matchings: Matchings, Matchings and Coverings in Bipartite Graphs, Perfect Matchings. Edge Colourings: Edge Chromatic Number, Vizing’s Theorem

UNIT IV

Independent Sets and Cliques: Independent sets, Ramsey’s Theorem, Turan’s Theorem. Vertex Colourings: Chromatic Number, Brook’s Theorem, Chromatic Polynomials.

UNIT V


Suggested Reading:

2. Douglas B West, Introduction to Graph Theory, Prentice Hall, 2004
CS5362  LOW POWER VLSI DESIGN

Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks

Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I
Introduction and need of low power design, sources of power dissipation, MOS transistor leakage components, SOI technology, FinFET, Back gate FET, power and energy basics, power dissipation in CMOS circuits, Energy-delay product as a metric, design strategies for low power.

UNIT-II

UNIT-III

UNIT-IV

UNIT-V

Suggested Reading:

CS5363 RELIABILITY AND FAULT TOLERANCE

Credits: 3

Instruction: (3L) hrs per week  Duration of SEE: 3 hours
CIE: 30 marks  SEE: 70 marks

UNIT-I

Introduction to Reliability Engineering: Reliability, Repairable and Non-repairable Systems, Maintainability and Availability, Designing, Reliability, Repairable and Non-repairable Systems, MTBF MTTF MDT, k out of in systems.

UNIT-II


UNIT-III

Software Reliability Modeling: Introduction to Software Reliability Modeling, Parameter Determination and Estimation, Model Selection, Markovian Models, Finite and Infinite failure category Models, Comparison of Models, Calendar Time Modeling.

UNIT-IV


UNIT-V


Suggested Reading:

CS5364 PERFORMANCE EVALUATION OF COMPUTER SYSTEMS
Credits: 3

Instruction: (3L) hrs per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I

UNIT-II

UNIT-III

UNIT-IV

UNIT-V
Analysis of Computer Architectures:
Case I: Central Server Computer System
Case II: Multiple Server Computer System
Case III: Petri Net Example
Suggested Reading: